MODEL 1950

DUAL FLEXIBLE DISK UNIT

37544

Instruction Manual

Part Number 43211 January 1981

esi Manual

MP MASTER

MA30713

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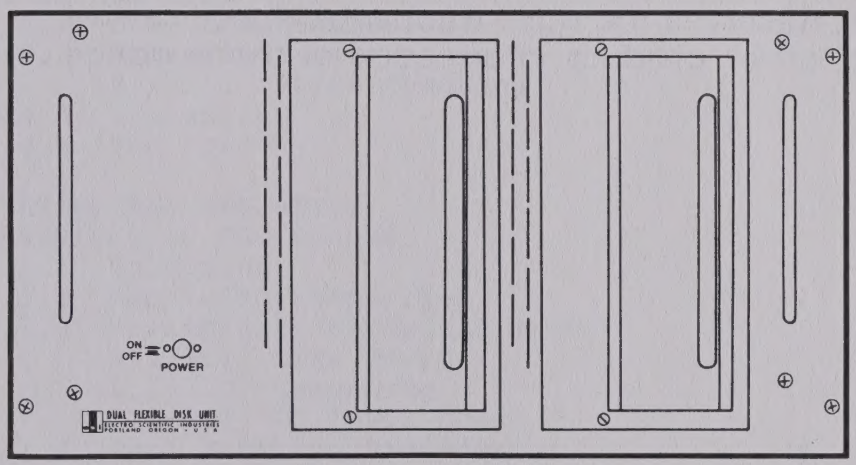

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SECTION 1
DESCRIPTION

1.1 GENERAL

The Model 1950 Dual Flexible Disk Unit is an auxiliary medium-capacity, random-access storage system specifically designed for PDP-11 digital computers, manufactured by Digital Equipment Corporation. The modular Model 1950 consists of an I/O card and up to four moving-head, compliant-disk recorders. One or two disk drive units can be mounted in a single chassis. Two chassis units are required for a system with three or four recorders.

The recording medium is an oxide-coated Mylar® disk enclosed in a plastic sheath. Each disk is easily changed for fast, convenient data storage or playback. Access to stored data is faster than conventional sequential recording media (such as magnetic tape) and the recording medium cost is held at a low level.

1.2 EQUIPMENT SUPPLIED

The Model 1950 is shipped with all equipment necessary for operation with PDP-11 minicomputer. The system consists of the following units:

1.2.1 Disk Recorder Chassis Unit(s)

Each chassis unit contains a power supply for one or two disk drives, a fan, the disk drive logic, disk formatter, the disk electronics, power switching controls, ac line cord and all internal cables. Slides and brackets are supplied for installation in a standard 19" RETMA rack.

For systems with three or four disk drive units, the one or two additional drive units supplied are in a second chassis unit, with a cable that interconnects the two chassis units.

1.2.2 Coupler Circuit Card

The coupler card fits into one of the I/O slots in the PDP-11 computer. It plugs into the computer main frame bus or expansion chassis bus, and controls the following functions:

Program interrupt
Device decoding
NPR control

Table 1-1. Model 1950 Specifications

Capacity per Disk	131,072 16-bit words (not including preamble or CRC words)
Number of Tracks	64
Number of Sectors	8 standard, with 16 also available
Words/Sector	256 data + 1 preamble + 1 CRC word
Rotational Speed	375 RPM
Access Time	10ms track-to-track
Settling Time on Last Track Moved	10ms
Data Transfer Rate	15.6 kilo words per second
Word Size	16 bits
Number of Drives Controlled	Up to 4
Mode of Data Transfer	NPR
Device Address	167200
I/O Slots Required	1
Size	(Approximately) 270mm x 490mm x 445mm (10,.5" H x 19.2" x 17.5" wide)
Operating Temperature Range	16°C to 35°C (60°F to 95°F)
Relative Humidity	20% to 80%
AC Power Requirement	115VAC, 50 or 60Hz, 5A; 230VAC optional
Weight	75 pounds (with 2 drives installed)

1.2.3 System Interconnect Cable Assemblies

The standard cable assembly consists of two cables. One connects the coupler circuit card directly to the recorder chassis. The other interconnects the formatter circuit and drive logic cards in the recorder chassis. A third cable is provided to connect the main recorder chassis to the optional recorder chassis for systems with more than two disk drives.

1.3 AVAILABLE SOFTWARE

Two standard programs are available for use with the Model 1950 and the PDP-11 series computers. The programs are briefly described below; for additional details, see Section 4.

1.3.1 Diagnostic Program

The diagnostic program verifies correct system operation, and provides a first level of fault isolation if malfunctions occcur. The diagnostic is also used to initialize new disks by writing header words and zeroing the data field on each sector of every track.

The diagnostic program 1) exercises all position and data transfer functions provided by the controller, 2) checks all status and error flags returned by the controller, 3) verifies proper operation of all units connected to the controller, and 4) checks that part of the computer interrupt system used by the controller. Some of the tests included in the diagnostic are designed to isolate errors which depend on the data content or mode of data transfer. Another set of tests is devoted to forcing error conditions and checking to see that they are properly reported by the controller. Tests are also provided to check for proper sector formatting and unit-to-unit compatibility.

1.3.2 Device Handler

A device handler compatible with the user's operating system will be supplied.

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 CONTROL FUNCTIONS

Each of the recorder chassis units is computer-controlled. Except for the line power switch operation and flexible disk loading, there are no operator actions required. For additional details on the recorder controls, see Section 3.

2.2 RECORDING MEDIUM

The Model 1950 Dual Flexible Disk Unit uses flexible magnetic disk cartridges, such as the Memorex FD/IV. The disk has a Mylar® substrate, and is coated with a magnetic iron oxide material. For protection, the disk is enclosed in a flexible vinyl envelope that is sealed around the edges, and lined with a self-cleaning wiper. The read/write head has access to the disk through an oval slot in the envelope. See Figure 2-1. One corner of the cartridge has a notch, which ensures that the cartridge is installed in the drive properly. To prevent further recording on the disk, a write-protect tab may be affixed to the cartridge. See Section 3.

2.3 RECORDING FORMAT

Each recorder chassis unit normally holds two disk drive recorder units for a maximum of four units within Model 1950 system. Each disk drive unit has a single moving-head recorder that will record up to 64 tracks on one side of a single disk. Each disk - and hence, each track - is divided into 8 sectors. The number of sectors may be changed to 16 by changing jumpers on the coupler card that plugs into the PDP-11 computer (See Section 3). In operation, each sector is identified by a sector hole, which is counted by electro-optical sensor logic from the index hole. The disk sector and track configuration is shown in Figure 2-2.

2.4 SECTOR FORMAT

2.4.1 General

The standard disk format has 8 sectors. On any track, each sector can store 256 user-accessible data words (16 bits each), plus non-accessible overhead words. The overhead words are added by the control logic to ensure disk interchangeability and synchronization.

The formats are listed in Table 2-1, which provides track capacity as a function of sector divisions. Note that if the overhead words are discounted, the track capacity per revolution is a constant (2560), which equals the product of the number of sectors and the words per data field. The sector format is shown in Figure 2-3, and described in the following paragraphs. Section 3 contains jumper wiring instructions for other formats.

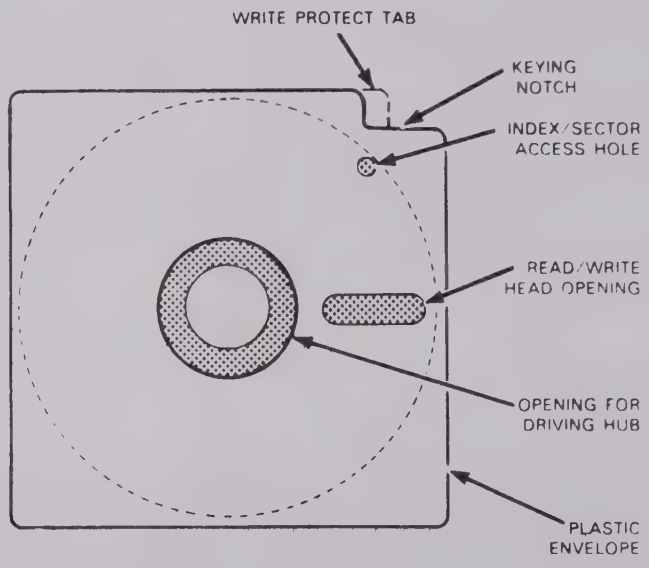


Figure 2-1. Disk Cartridge Configuration

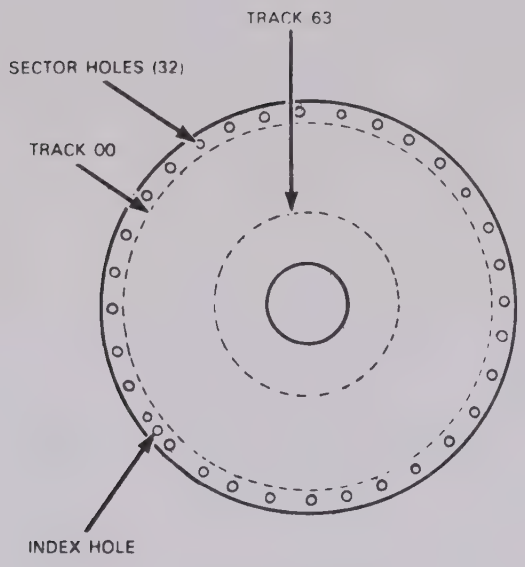


Figure 2-2. Disk Configuration and Recording Format

Table 2-1. Allowable Sector Configuration

Sectors	Data Words/Block Words/Sector	Number of Blocks
8	256	512
16	128	1024

Number of Tracks is 64.

2.4.2 Bit Synchronization

The bit sync field consists of a series of 128 data zeroes recorded at the beginning of the sector. It synchronizes the self-clocking circuit of the read data decoder, and ensures interchangeability between cartridges and disk drives. This field is not user-accessible.

2.4.3 Accessible Data

This field is user-accessible and its contents are not restricted. In the standard 8-sector recording format, this field can store 256 data words of 16 bits, which are recorded serially.

2.4.3.1 Error Checking

For checking data field errors Model 1950 uses a hardwired CRC error-checking polynominal, which has the form:

$$X^{16} + X^{15} + X^{2} + 1$$

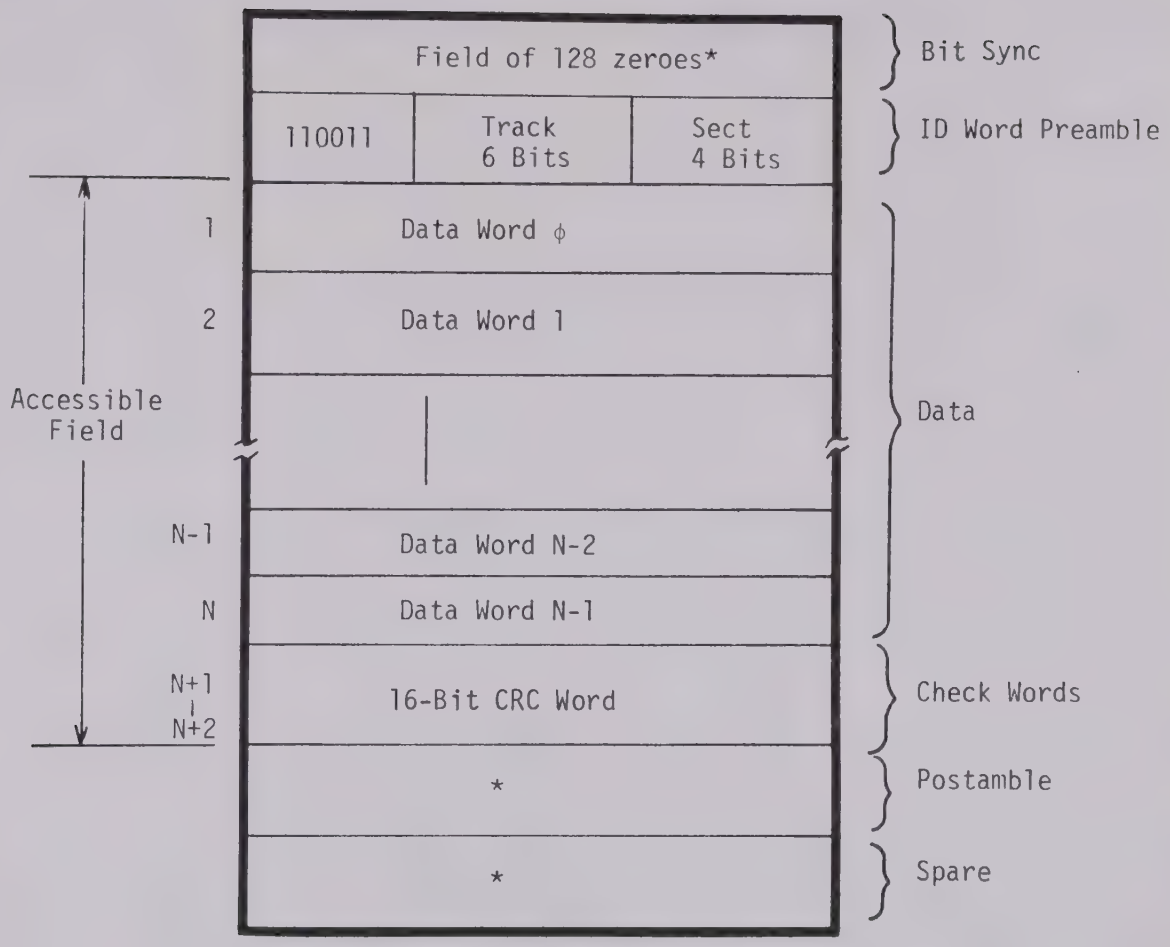
It is the industry standard and provides error checking for bursts of up to 16 consecutive dropouts.

2.4.4 Postamble

The hardware generates additional data after the last word of the accessible data field to ensure that no bit crowding exists on the last word of useful data. The postamble is not accessible by software.

2.4.5 End Space

Space at the sector end allows for worst-case speed variation, media tolerances, and drive-to-drive interchangeability.



* Not under software control.

Figure 2-3. Model 1950 Sector Format

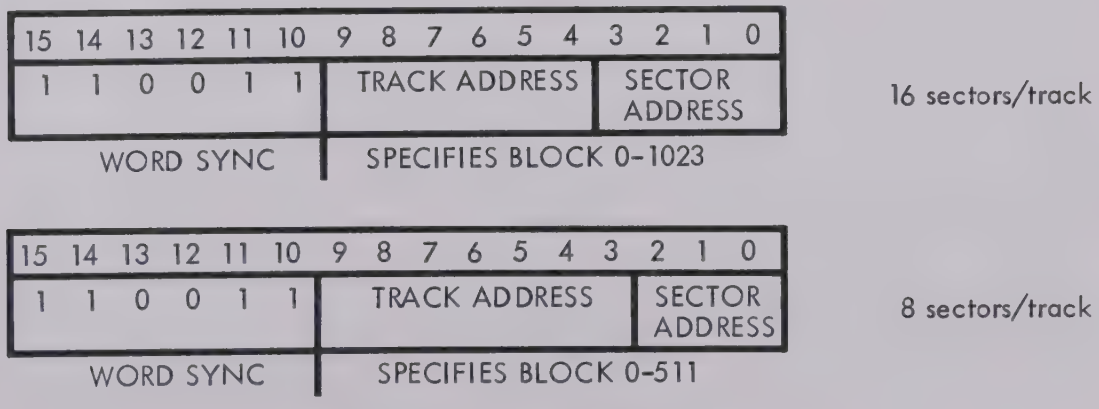

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 1 0 0 1 1
TRACK ADDRESS
SECTOR ADDRESS
WORD SYNC
SPECIFIES BLOCK 0-1023
16 sectors/track
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 1 0 0 1 1
TRACK ADDRESS
SECTOR ADDRESS
WORD SYNC
SPECIFIES BLOCK 0-511
8 sectors/track

Figure 2-4. ID Word Formats

SECTION 3

INSTALLATION AND OPERATION

3.1 INSTALLATION PROCEDURES

3.1.1 Unpacking

1. Cut the tape securing the top of the shipping container; be careful not to cut deeper than is necessary to cut the tape.

2. Remove and save box on top of the unit; it contains the coupler card, cables, etc.

3. Remove the rack mount slides from the top of the unit, and the manual and disk packs from the sides of the unit.

4. Lift the unit and the foam shipping pads from the box.

5. Remove the foam shipping pads and the plastic sheet from the unit.

6. Remove the coupler card, cables, etc. from the box that was on top of the unit.

7. Replace all foam pads, plastic sheets, box and other packing materials in the shipping containers and save. If the unit is to be reshipped (e.g., for factory service), it must be shipped in this container to avoid shipping damage. See Section 3.3 for repacking instructions.

3.1.2 Receiving Inspection

1. Remove the unit from the plastic bag and inspect for shipping damage. If any damage is noted, contact the shipping carrier immediately to file an insurance claim.

2. Check all system components against the configuration sheet, which was taped to the top of the box containing the control card and cables. Report any missing items immediately.

3. Loosen the screws on both sides and the back of the chassis and remove the top cover. It is not necessary to remove these screws.

4. Check the chassis interior to ensure that all screws are tight, the printed circuit cards are secure, the internal cables are in place, and the interior and exterior fuses are in place.

3.1.3 Preliminary Setup and Tests

This test verifies that the power supply is operational and that the recorders are properly connected.

3.1.3.1 Line Power

Model 1950 system is designed for operation on 115VAC, 50 to 60Hz, single phase line power. Do not attempt to convert the Model 1950 System for 230V operation. Line power is supplied via a single power input cable to each recorder chassis in the system. Maximum current is 5 amperes per chassis unit.

3.1.3.2 Grounding

All chassis units are equipped with a standard 3-wire power cable that connects the chassis to earth ground when plugged into the appropriate receptacle. For use with a 2-contact receptacle, use an adapter and connect the third (ground) lead to earth ground.

3.1.3.3 DC Power Check

Plug in the line power cord at the rear of the chassis, and then connect the cord to the appropriate ac receptacle. Do not connect any other cables to the chassis, and do not place any disk in the drive. Turn front panel POWER switch to ON. If POWER indicator light is ON, the power supply is operational. If indicator is not ON, check for:

Blown fuse
Burned-out bulb
Defective power supply

WARNING

ALWAYS DISCONNECT THE 115VAC LINE POWER WHEN CHECKING OR REPLACING POWER SUPPLIES OR FUSES WITHIN THE CHASSIS UNIT.

Check the power supply voltages and fuses. Power supply voltages can be checked on the power supply PC board. These voltages are with respect to chassis ground. See Figure 1-1 for test locations. If these voltages do not match those in Table 3-1 the unit should be returned to the factory for repair. See Paragraphs 6.4 and 6.5.

Supply	Voltage Tolerance
+5V	+Ø.3 to -Ø.2
+24V (Unregulated	+5.Ø to -Ø
-12V	+2 to -Ø.5

Table 3-1. Power Supply Voltages

Supply	Rating (Amps)
Rear Panel AC	5
-12VDC	3
+5VDC	1Ø
+24VAC	5

Table 3-2. Supply Fuses

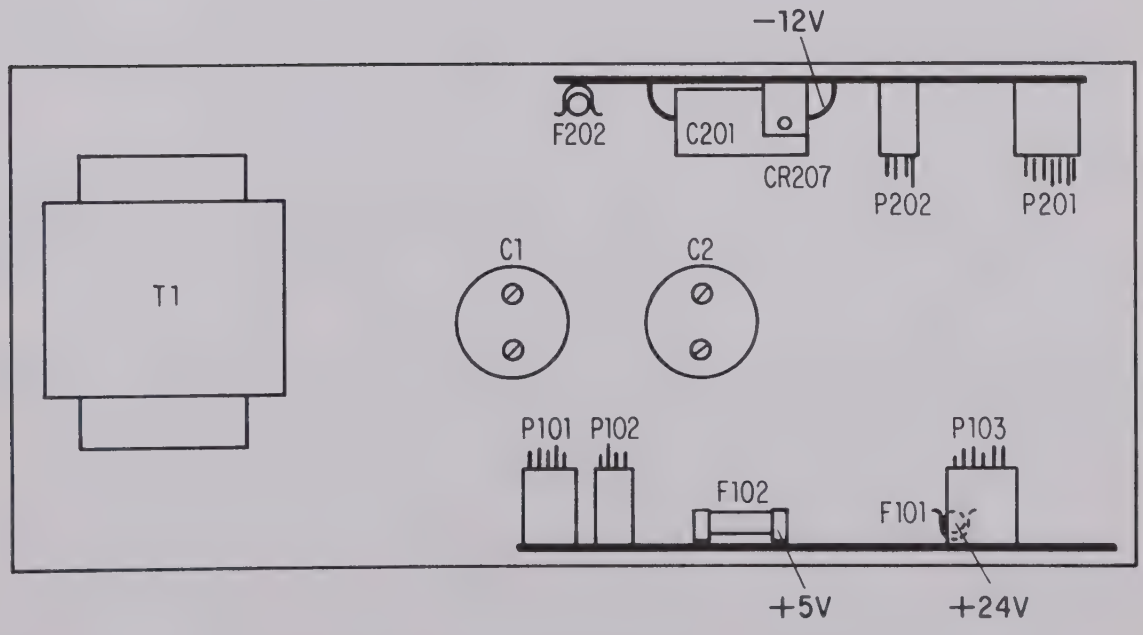


Figure 1-1. Voltage Test Locations

3.1.4 Rack-Mounting Procedure

1. The Model 1950 chassis unit(s) are normally mounted in a standard 19" rack; all necessary mounting hardware is supplied. During installation, be sure that the chassis units are close enough to the computer so that the cables are not subject to unnecessary stress when the chassis units are extended from the rack for service. Allow at least 2-1/2 feet of cable slack.

2. Separate the chassis slide and mount it on chassis. Use the 10-32 x 3/8" screws supplied.

3. Attach the rear slide mount bracket to the rear tapped rail. The center line of the bracket will be 5.25" below the top of Model 1950 chassis when installed. Use 10-32 x 3/8" screws.

4. Attach the front slide mounting bracket to the inside of the front tapped rail with 10-32 x 3/8" screws.

5. Connect the rear extension bracket to the back end of the cabinet slide section with 10-32 x 3/8" screws and nuts.

6. Before Model 1950 is inserted in the cabinet, back out the pawl fasteners to their full extension by turning the right-hand pawl fastener fully CCW, and the left-hand fastener fully CW.

7. Extend the cabinet slide sections fully, until they are locked.

8. Slide the chassis onto the extended slide sections. Release the locks as the unit is pushed forward.

9. Push the unit forward until the front panel is in contact with the tapped rails. It may be necessary to loosen the screws holding the slides to the tapped rails, to allow the unit to center. Be sure to tighten the screws after centering.

10. When all adjustments are complete, tighten pawl fasteners to retain chassis in cabinet.

3.1.5 System Interconnection

Model 1950 uses flat, flexible cables. The coupler card connector plugs directly into wire wrap pins. The recorder chassis connectors plug directly onto the edge connectors of the formatter and drive logic drive PCB's. The cables are connected through slots in the chassis. If only one recorder chassis is used, connect the coupler to J3 on the recorder chassis. Use the short jumper cable to connect J4 to J2. If a second recorder chassis is used, connect J1 of the main recorder chassis to J2 of the second chassis.

3.1.6 Coupler Card Installation

If the coupler card is to be used with non-standard priority, address or format, wiring changes will be required before installation. These changes are outlined in Section 3.1.7. For standard operation in a PDP-11 computer, proceed as follows:

3.1.6.1 I/O SLOT Selection

Model 1950 coupler can be installed in any available small peripherial controller (SPC) slot in the PDP-11 main frame or extender chassis. Since the 1950 is an NPR device, the NPG jumper associated with the chosen slot must be removed. This is a wire-wrap jumper located on the backplane between pins CA1 and CB1 of the chosen SPC slot. Note that if the coupler card location is changed at a later date, this jumper must be replaced.

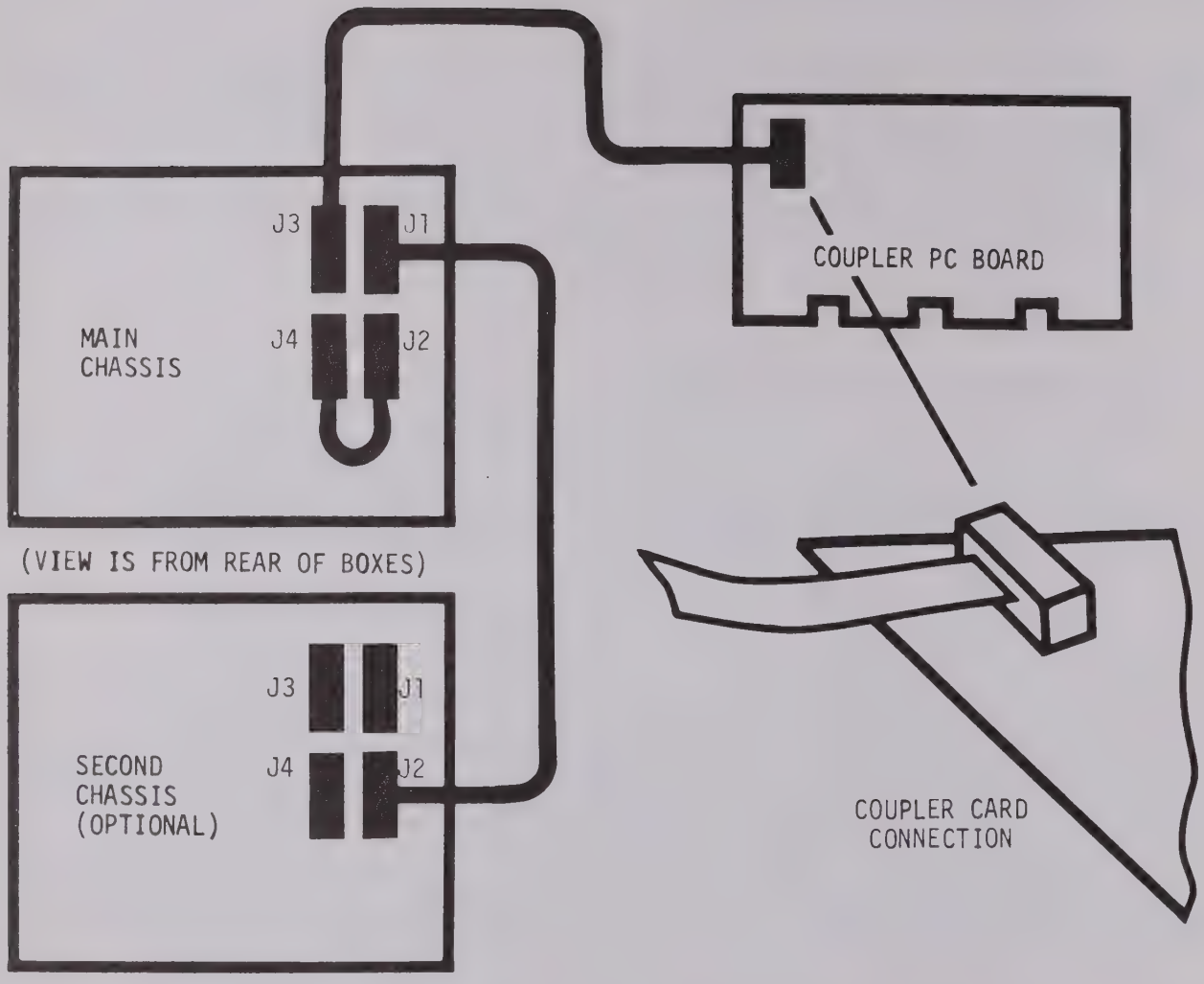


Figure 3-2. Cable Interconnection

3.1.6.2 Coupler Card Plug-in

Install the coupler card into the selected I/O slot. Be sure the edge connectors are properly positioned before seating the board. This will prevent damage to the connectors. Dress down the cable. Keep the cables to the various I/O boards neatly packed.

3.1.7 Coupler Card Modifications

To modify the device address or the interrupt vector address, certain wiring trace changes must be made on the coupler.

3.1.7.1 Device Address Modification

The device address for the Model 1950 has six octal digits which are normally set for 167200. This address can be changed so that the address is 16X1X2X30 where X1, X2 and X3 are all selectable. Figure 3-3 illustrates the change locations for X1 and Figure 3-4, the locations for X2 and X3. To change the address, cut the appropriate traces and reconnect the correct zeroes and ones to the out pads.

3.1.7.2 Vector Address Modifications

The vector address for the Model 1950 has three octal digits, which are normally set for 140. All digits are selectable. Assuming they are of the form X4X5X6, Figure 3-5 illustrates the change locations. For digit X6, only the MSB is selectable.

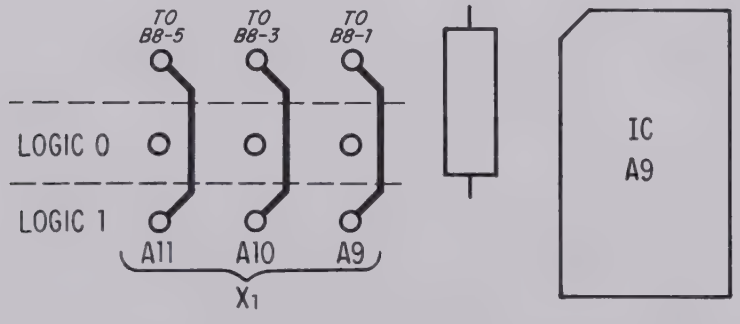


Figure 3-3. Changes for Address Digit X1

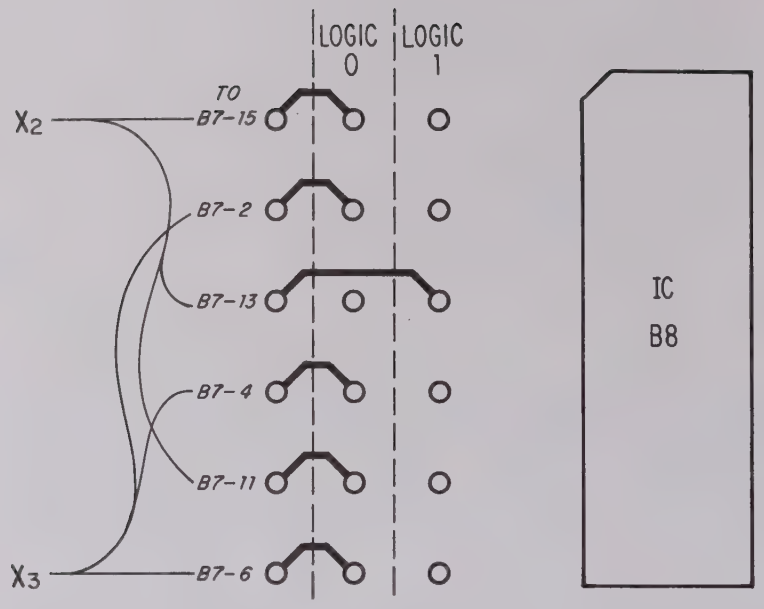


Figure 3-3. Changes for Address Digits X2 and X3

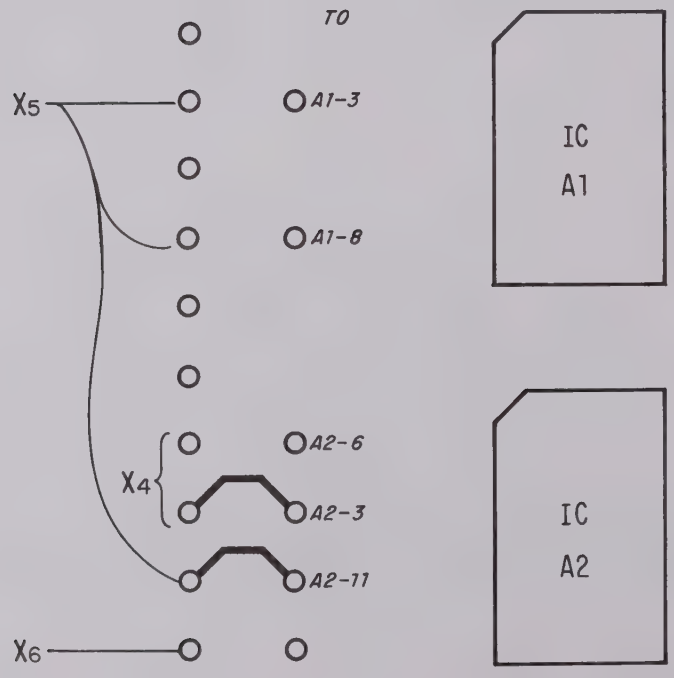


Figure 3-4. Changes for Vector Address

3.1.8 Format Modifications

The Model 1950 is normally supplied with 16-bit words, 8 sectors and 256 words/sector/track. These can all be changed by proper connection of four jumpers provided on the formatter PCB in the recorder chassis. The jumpers are:

Jumper	Pin
12-Bit	S/B K2-5
OS	H3-12
16-Sector	H4-2
8 Bit	H4-1

These jumpers are activated when the pins are jumped to ground. Their effect on the format and word size is given in Table 3-3.

Jumpers Activated	Word Size	Number of Sectors	Words/ Sector	Coupler Card Format Jumper
12 Bit	12 Bit	10	256	10 Sector
12 Bit • OS	12 Bit	8	320	8 to 16 Sector
12 Bit • OS • 16 Sect	12 Bit	16	160	"
8 Bit	8 Bit	16	256	"
16 Sect	16 Bit	16	128	"
No Jumpers*	16 Bit	8	256	"

*Standard for PDP-11.

Table 3-3. Word and Sector Formats

3.2 OPERATING INFORMATION

3.2.1 General

After Model 1950 is installed, operation consists of loading the appropriate software, loading the disks, and turning the power ON to the chassis unit(s). Software instructions are included in Section 4; the operating information in this section covers disk loading instructions (Section 3.2.2) and the control and indicator operating information (Table 3-4).

3.2.2 Disk Loading and Handling

3.2.2.1 General

Each flexible disk is enclosed in a plastic jacket. Wipe cushions are bonded to the inside of the jacket, so that the disk is housed and rotates between the cushions. To insert a disk in the recorder unit, open the door, slide the disk all the way into the guide. Do not close the door (see Figure 3-6). Turn the disk drive on before closing the door. This ensures proper registration of the disk. When the disk is in place and the disk drive on, close the door slowly to engage the drive spindle.

3.2.2.2 Disk Interchangeability

To ensure interchangeability, store the disks in a location that is within ±5°F of the using system ambient temperature, and within ±10% of the using system humidity. Disks stored outside these ranges must be placed in the using system environment at least 20 minutes prior to use.

Control	Function
POWER	Alternate-action pushbutton switch and indicator lamp. Depress to turn ON chassis unit line power. When power is ON, indicator lamp and fan are both on. Depress again to turn line power OFF.

Table 3-4. Model 1950 Controls and Indicators

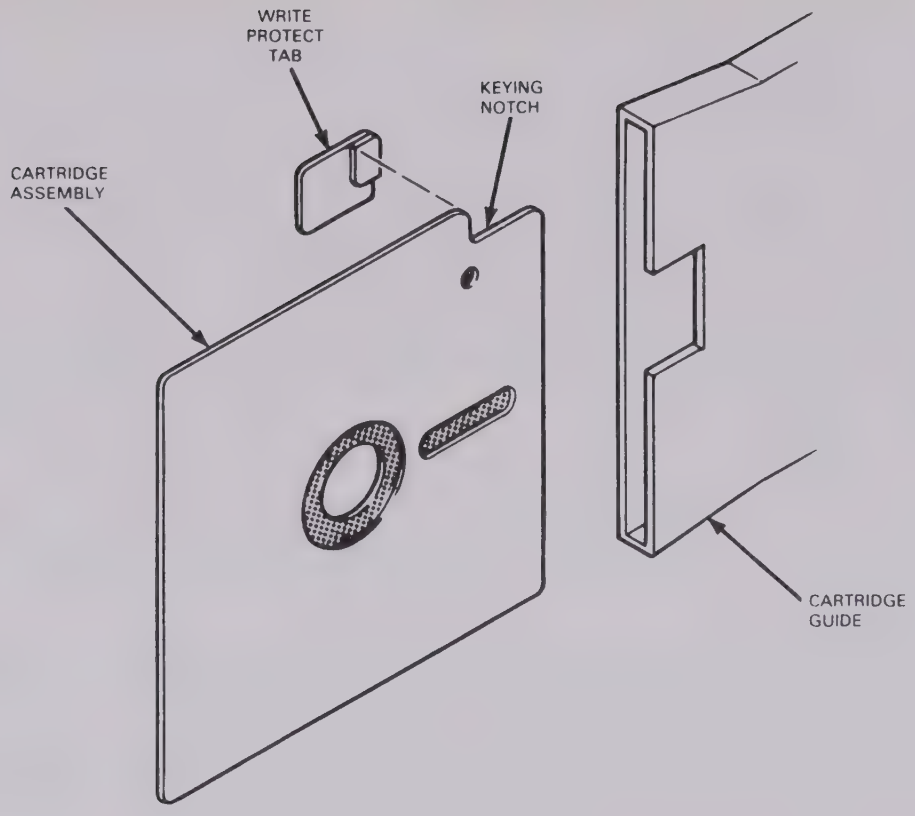


Figure 3-6. Insertion of Disk Cartridge in Guide

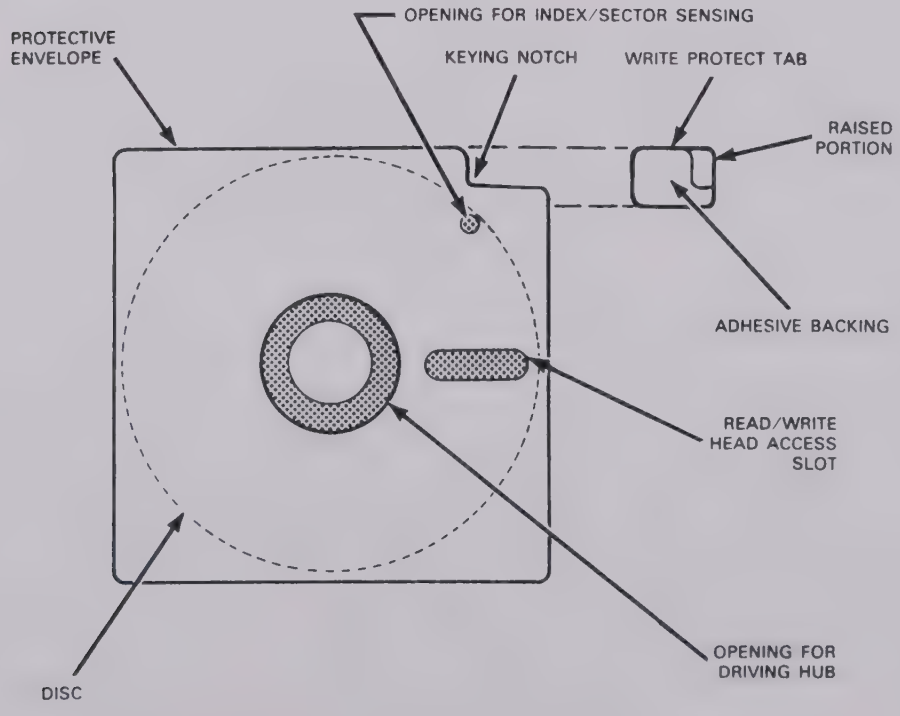


Figure 3-7. Write Protect Tab Insertion

3.2.2.3 Disk Precautions

After removing a disk from the recorder, it should be stored in a plastic-coated paper envelope. To protect the disk, use the same care and handling procedures specified for computer magnetic tapes. For best results, observe the precautions in Table 3-5 below.

1.	Return the disk to its storage envelope whenever it is removed from file.
2.	Store disks vertically.
3.	Keep disks away from magnetic fields and from ferromagnetic materials that might become magnetized. Magnetic fields greater than 50 Oersteds can distort recorded data on the disk.
4.	Replace storage envelopes when they become worn, cracked, or distorted.
5.	Do not write on the plastic cartridge. Writing pressure may damage the disk.
6.	Do not smoke while handling disks. Heat and contamination from a carelessly dropped ash can damage the disk.
7.	Do not expose disks to heat or sunlight. The recorder read/write head cannot properly track a warped disk.
8.	Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

Table 3-5. Disk Handling Precautions

3.2.2.4 Disk Write Protection

To inhibit writing on any disk, remove the covering on the plastic write-protect tab, and slide the tab into the keying notch of the vinyl envelope containing the disk (Figure 3-6). The tab is removable. With the tab in position, and the disk in the drive unit, the raised portion of the tab pushes an actuator that closes the write-protect switch, and the drive unit does not write. To restore the full read/write operation, remove the write protect tab from the disk.

3.2.3 System Start-up/Performance Test

3.2.3.1 General

Following installation and turn-on, the system should be given a thorough performance check. Use tests 1 through 17_8 of the Flexible Disk Diagnostic. Section 4 has a description of the diagnostic, and instructions for performing the diagnostic. The diagnostic will test and verify correct operation of the mechanical system, interconnections, and electronic system.

3.2.3.2 New Disk Initialization

Each time a new disk is used in the Model 1950 system, it must be formatted or initialized. Formatting consists of running diagnostic tests 1 through 3 before using the disk in the system. On disks that have been strongly degaussed, test 1 should be run three times before tests 2 and 3 are run, to ensure that the disks are properly formatted. See Section 4 for the diagnostic procedure.

3.3 PACKING INSTRUCTIONS

If the Model 1950 is to be shipped by common carrier, use the original container and pack it according to the following procedure:

1. Remove Model 1950 chassis unit(s) from the rack, and take off the chassis half of the slide rails prior to packing.

2. Wrap Model 1950 in a plastic sheet to prevent scratching.

3. Place Model 1950 chassis unit(s) in foam pads and place the chassis and pads in the container. Note that there is a right-hand and a left-hand pad; the cutout goes to the bottom of the chassis unit.

4. Put manuals on the side next to the chassis unit. Wrap the rackmount slides in cardboard and place them on top of the chassis unit.

5. Place the PC cards, cables, etc. in the cardboard box, and seal with tape. Place the box on top of the foam pads. Seal the box, even if it's empty, and place it on top of the chassis as filler for the shipping container.

6. Close the shipping container and seal it with glass-reinforced paper tape.

SECTION 4
SOFTWARE DATA

4.1 SCOPE

The following section describes Model 1950 Input/Output instructions for users wishing to write their own drivers (including programming examples). Also included are descriptions of disk diagnostic programs.

4.1.1 Special Symbols

The following special symbols are used throughout the remaining portion of this manual to help clarify the examples pertaining to the users response (typed input) to the computer terminal.

↵	Carriage return. Indicates that the user is to depress the RETURN key on the terminal keyboard.
↑	Up arrow. Terminal display or printout indicating that the CTRL (control) key on the terminal keyboard was held down while typing a following character. (Examples: ↑W, ↑X, ↑Y, ↑T, ↑L, ↑C, etc.) The carriage return (↵) is not required when the CTRL key is used.
␣	Space. Symbol is used only initially to indicate where the user is to type a mandatory space between data entries.

4.2 PROGRAMMABLE REGISTERS

The Model 1950 is a programmable register oriented device; which simply means that all operating functions and features are controlled by registers accessible to the operating program. Not all of the programmable registers can transfer information in both directions. Of the four registers accessible to the program two are Write Only, one is Read Only and one is Read/Write.

Register	Address	Symbolic
Command (WO)	167200	CM
Status (RO)	167200	ST
Disk Address (WO)	167204	DA
Memory Address (RW)	167202	MA

The general procedure for loading a register is:

MOV src, XX where XX is the symbolic address.

The general procedure for reading a register is:

MOV XX, dst where XX is the symbolic address.

4.2.1 Model 1950 PDP-11 Input/Output Instructions

The detailed input/output instructions are included below for users wishing to write their own drivers.

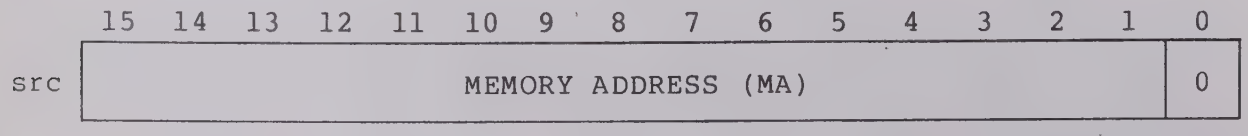
Input/Output Instructions Summary

Operation Mnemonic	Symbolic	Operation
LDCM	MOV src, CM	Load command word
LDMA	MOV src, MA	Load memory address
LDDA	MOV src, DA	Load disk address
RDST	MOV ST, dst	Read disk status
RDMA	MOV MA, dst	Read memory address

The instruction order for read or write operations is LDMA-LDDA-LDCM; for a seek operation the order is LDDA-LDCM, and for a check is LDDA-LDCM.

4.2.1.1 Load Memory Address - LDMA - MOV src, MA

Loads the formatter memory address register from src Ø-15 with the starting address for data transfers. This instruction must not be executed while BUSY is set.



If the extended memory feature is used the memory extension bits are contained in the command word.

4.2.1.2 Load Disk Address - LDDA - MOV src, DA

Loads the formatter disk address register from src, as appropriate for 8 or 16 sector format, with the unit number, track number and sector number. This instruction must not be executed while BUSY is set or if the selected unit is Seeking.

16 Sector Format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
src					UNIT		TRACK						SECTOR			
					U1	U0	T5	T4	T3	T2	T0	T0	S3	S2	S1	S0

8 Sector Format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
src					UNIT		0	TRACK						SECTOR		
					U1	U0		T5	T4	T3	T2	T1	T0	S2	S1	S0

Bits 11-10 Unit Select - UN

Select	Unit
00	Unit 0
01	Unit 1
10	Unit 2
11	Unit 3

The value of UN selects the disk unit on which the operation specified in the command word is to be performed.

Sectors may be regarded as arranged in sequence from track 0 through track 63, so that the combined track and sector number select one sector from 1024 (16 sector format) or one sector from 512 (8 sector format).

4.2.1.3 Load Command Word - LDCM

Loads the formatter command register with the command in src 0-7. The instruction clears certain controller status flags, sets BUSY, and initiates the operation specified by the OP Code bits. When the operation has been completed BUSY is reset, and if interrupts are enabled, an interrupt occurs. This instruction must not be executed while BUSY is set.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
src	0	0	0	0	0	0	0	0	C	R	I	ME		$H/_F$	OP	

Bits 1-Ø	Op Code	Operation
	ØØ	Read
	Ø1	Write
	1Ø	Check
	11	Seek/No-op

A detailed description of the various operations is given in Section 4.

Bit 2	H/F	Half Sector/Full Sector
	Ø	Read or Write one full sector
	1	Read or Write one half sector
Bits 4-3	ME	Memory Extension
	ØØ	A17 = Ø, A16 = Ø
	Ø1	A17 = Ø, A16 = 1
	1Ø	A17 = 1, A16 = Ø
	11	A17 = 1, A16 = 1
Bit 5	I	Interrupt Enable
	Ø	Disable Interrupts
	1	Enable Interrupts
Bit 6	R	Restore
	Ø	Seek directly to track address
	1	Restore to home position before seeking to track address
Bit 7	C	Check Character
	1	Read or Write the check character (CRC)
	Ø	Do not Write or Read CRC

4.2.1.4 Half Sector Full Sector (Bit 2)

If this bit is set for a Read or Write operation, a half sector of data is transferred as follows:

Write: A half sector of data is transferred starting at MA and the remainder of the sector is zeroed (padded with zeroes).

Read: A half sector of data is read into a buffer starting at MA.

For 16 sector and 8 sector formats, half sectors correspond to 64 and 128 words respectively.

Half sector operations are incompatible with reading or writing the check character (refer to Section 4.2.3).

4.2.1.5 Memory Extension Bits (Bits 3-4)

These two bits in conjunction with the memory address register are used to express an 18-bit absolute memory address for NPR data transfers (DMA). The bits are redundant if the particular PDP-11 is not equipped with the extended memory feature.

4.2.1.6 Interrupt Enable (Bit 5)

If this bit is set and the operation causes BUSY to set, then when the operation has been completed and BUSY is reset, or if an error condition resets BUSY, an interrupt occurs. This means that a Seek/No-op operation cannot generate an interrupt.

The computer will not detect the interrupts if the system interrupts are disabled.

4.2.1.7 Restore to Home Track (Bit 6)

If this bit is set, the selected unit automatically seeks to the home position. Any additional seeking (as specified in the Disk Address Register) is then performed.

BUSY is set if the rest of the command (Op code) so stipulates, otherwise BUSY is unaffected.

4.2.1.8 Read/Write Check Characters

If this bit is set when a Write operation is specified, an additional 2 words, containing the check (CRC) character and a word of zeroes are appended to the data block. If there are n words per sector, then words 0 through n-1 contain data and word n and n + 1 of the memory should contain the check character and words of all zeroes.

If this bit is set when a Read operation is specified, the nth and (n+1)st (containing the check character and one word of zeroes) is transferred into the memory buffer after the data words of the sector.

Reading or writing the check character is incompatible with half-sector operations, and should not be attempted.

4.2.2 Read Disk Status - RDST - MOV ST, dst

Loads dst 0 - 10 and 12 - 15 with the disk operating and error status and loads dst 11 with the BUSY flag. Note that dst will contain the status of the unit last selected by an LDDA instruction. The instruction (RDST) may be executed when BUSY is set, but the status indicators may not be current.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dst	ERROR	FATAL	BUS ERR	SEEK	BUSY	I	ME		NRDY	TOE	WPE	FE	RE	PCE	CRCE	SEEK

Bit 7 NRDY — Not Ready
Signified that the selected unit cannot accept any valid command. The reason may be that the disk is not up to speed, a disk is not in place, or the disk is not powered up.

Bits 9-8 ME — Memory Extension Bits
These two bits show the state of the memory extension bits (A17 - A16), as specified by the command word.

Bit 10 I — Interrupt Enable
This bit signifies whether or not the interrupt enable bit in the command word is set.

Bit 11 BUSY — This bit is set when the formatter is BUSY. The formatter goes busy for a write, read or check operation. It is reset on the completion of such operations, or when certain errors occur. BUSY is not set when a Seek/No-op command is executed.

Bit 12 SEEK — Same as bit 0.

Bit 13 BUS ERR — Bus Error
A bus error occurs when there is no response from the CPU to a formatter NPR request. This may occur when the memory address register contains a non-existent memory address, or an address not assigned to data storage.

Bit 14 FATAL — Fatal or Premature Termination Error
Signifies that the operation was either prematurely terminated, or that a non-recoverable error condition occurs. This flag is an OR of WPE, TOE and FE.

Bit 15 ERROR — This bit signifies that any of the listed error conditions has occurred - fatal or otherwise.

Note that all of the fatal errors cause BUSY to reset immediately when the error condition is detected. If interrupt is enabled the interrupt will still occur.

4.2.3 Operating Modes

4.2.3.1 Read Operation (OP = 00)

Causes the formatter to input data from the specified sector on the selected unit directly to computer memory (DMA). Either one full or half sector of data is read from the sector specified by the Disk Address Word into a buffer at start address MA.

When the command word is loaded BUSY is set, a seek to the track given in the Disk Address is initiated, and the Seek indicator of the status word is set until the seek is complete. If the Restore bit (R) is set, the read/write head on the selected unit first seeks to track 0 and then the seek to the selected track is initiated. In either case the Seek indicator is set until head motion stops.

During each read operation, the sector preamble is automatically hardware compared and the check character is calculated over each data word in the sector (regardless of how many words are transferred). The check character is then hardware compared against the check character generated during the last write operation on the sector.

BUSY is set when the command word is loaded, and is reset after all the words specified (full or half sector) have been transferred, and the check (CRC) character has been compared. If the interrupt bit (I) is set when the command is loaded, an interrupt occurs when BUSY resets. If the C bit of the command word is set the check (CRC) character is transferred into the memory buffer.

Bit 0	SEEK	The unit currently selected is seeking or restoring. If BUSY is reset, this indicator is considered an error, unless the last operation was a Seek/No-op.
Bit 1	CRCE	CRC Error or Check Character Compare Error The check character calculated during the last Read or Check operation did not match the one previously written on the sector.
Bit 2	PCE	Preamble Compare Error During the last Read or Check operation, the sector preamble at the beginning of the sector was not what it should have been. No data transfer occurs.
Bit 3	RE	Rate Error Data was not supplied or accepted by the CPU within the time restraints of the data transfer rate. BUSY is immediately reset at the time the error occurs.
Bit 4	FE	Format Error During a write, read or check operation, an end of sector was detected before the specified operation was completed. This error could occur if 8 sector format operations were specified on a disk formatted for 16 sectors.
Bit 5	WPE	Write Protect Error A write operation was terminated because the disk in the selected unit was write protected; or certain fault indicators have been detected within the drive itself.
Bit 6	TOE	Timeout Error The last operation was not completed because the specified sector address was not found within 2.5 seconds. This error can occur by specifying a non-existent sector address or by a hardware malfunction.

4.2.3.2 Write Operation (OP = 01)

Causes the formatter to output data from the computer to the selected unit. Either one full sector or one half sector of data is written from a buffer beginning at the address specified by the memory address register and the memory extension bits. The data is transferred to the sector specified by the Disk Address.

The formatter goes BUSY when the command word is loaded and a seek to the track given in the disk address word is initiated. The Seek indicator in the status word is set and remains set until head motion stops. If the Restore bit (R) in the command word is set, the read/write head on the selected unit is first restored to track 0, before the seek to the selected track is initiated.

During a write operation the sector preamble is automatically rewritten by the formatter. The check character is calculated over each word of the sector (regardless of whether a full or half sector is written). If a half sector of data is written, the remaining half of the sector is automatically padded with zeroes. Nonetheless, the check character is still calculated over each word of the sector. If the CRC or check character bit of the command word is set the CRC character from memory is appended to the data block.

BUSY is set when the operation is initiated. When all the words (full or half sector) have been transferred and the check character has been generated BUSY is reset. If interrupts are enabled (bit I of the command word), an interrupt occurs when BUSY resets.

4.2.3.3 Check Operation (OP = 10)

Causes the formatter to compare the preamble and check words on a selected sector without transferring data. The sector address is given by the Disk Address word.

When the command word is loaded BUSY is set and a Seek to the track specified by the Disk Address is initiated. The Seek indicator in the Status Word is set and reamins set until head motion stops. If the Restore bit (R) in the command word is set, the read/write head on the selected unit is first restored to track 0, before the seek to the selected track is initiated.

During each check operation, the sector preamble is automatically hardware compared, and the check character is calculated over each data word in the sector. The calculated check character is then hardware compared against the check character generated during the last write operation on the sector. A full sector is always checked, independently of the H/F bit in the command word.

BUSY is set when the command word is loaded and reset when the sector has been checked. If interrupts are enabled an interrupt is generated at the time BUSY resets.

4.2.3.4 Seek/No Op (OP = 11)

Causes the formatter to select the unit specified in the Disk Address Word and to position the read/write head to the track specified in the Disk Address Word. This operation is used primarily as a unit select operation, to either effect a Restore or as a preliminary to reading the status of the selected unit.

When the command word is loaded, a Seek to the selected track is initiated and the seek indicator in the Status Word is set and remains set until head motion stops. If the Restore bit (R) in the command word is set, which is usually the case, the read/write head is restored to track 0, before the seek to the selected track is initiated. The selected track number is usually 0.

BUSY is not affected by this operation and there is no checking of the sector specified in the Disk Address. No data is transferred and no preamble is written. The check bit in the command word is ignored during this operation.

4.2.4 Programming Hints and Suggestions

The following information is provided to assist the user in preparation of disk operating programs with regard to general procedures, preliminary status checks, error checking and error recovery.

4.2.4.1 Initiation of an Operation

Every new operation should start with a Seek/No-op as a means of selecting a particular unit and as an introduction to reading the subject units status. Certain preliminary status checks should be carried out to determine if the unit can currently execute the proposed operation.

Having determined that the unit is operationally capable of executing the operation the general order of initiation is as follows:

1. Load the memory address register MA, with the start address of the input or output buffer (read or write operations only).

2. Load the Disk Address word (unit, track, sector). This step is not necessary for a Seek/No-op operation if the read/write heads are to be restored.

3. Load the command word. Enable interrupts for read, write or check operations as required. Specify full or half sectors as required. Configure the memory extension bits to suit either 16 or 18-bit memory addressing as dictated by the start address of the input or output buffer. Set or reset the check character bit (C) as suited to the operation (read or write); noting that in a read operation the check character will be the last character transferred to the input buffer and in a write operation the check character must be supplied from the last character position of the output buffer. Note also that enabling the check character bit is not compatible with half sector transfers. Set the Restore bit as required, remembering that the initial seek is to track 0 and then to the specified track.

4.2.4.2 Preliminary Status Checks

As a simple means of retrieving the subject units status, load the Disk Address word; this selects the unit without affecting any other action, then read the status (MOV ST, dst).

The first check for all operations is to determine that the unit is ready to accept a valid command; i.e. the Not Ready indicator (NRDY) is reset. If this indicator is set some form of "device attention" is required.

If the unit is BUSY, perform some other operation on a different unit, or, go into a BUSY test loop (wait for NOT BUSY). As a general rule do not issue any command to a BUSY unit. The status of a BUSY unit is not current.

If the selected unit is seeking, go into a Seek test loop (wait for Not Seeking), or, perform an operation on a different unit. It is possible to have operations on different units running concurrently, e.g., two units seeking while one is reading or writing.

If the proposed operation is a Write, check that the unit is not file protected.

4.2.4.3 Error Checking

On completion of an operation the status is immediately available to the operating program (RDST), whether completion is indicated by an interrupt, or a test for NOT BUSY.

The first check should be to determine if there has or has not been an error (bit 15 of the status word). If the Error bit = 0 no further checking need be carried out and the operation can be assumed

successful. If the Error bit = 1, then the nature of the error should be determined, i.e. fatal or otherwise (bit 14). If bit 14 = 1 a fatal error is indicated, and will be one of TOE, WPE and FE. These errors are non-recoverable and should be treated as follows:

TOE. Check that the track and sector address used in the current operation is valid, i.e., that it exists.

WPE. The preliminary status check for this unit ignored the write protect flag, or the wrong status was read.

FE. An obvious reason for this error is that 8 sector word transfers (256) were attempted on a 16 sector formatted disk (128 words).

If bit 14 = 0 the errors are considered recoverable. These errors are PCE, CRCE, and RE. Of these errors the error checking procedure should first check for a Rate Error (RE) since the absence of PCE and CRCE errors does not mean that a Rate Error cannot occur on its own (the absence of data errors is no compensation for a rate error). The last two errors are considered as data errors and may be checked in either order. If a rate error occurred there is no point in making data error checks.

4.2.4.4 Simple Error Recovery Procedures

As previously stated the recoverable errors are: Preamble Compare Error (PCE), CRC or Check Character Error (CRCE), and a Rate Error (RE).

For these errors the recommended procedure is:

1. Three in-place retries of the operation in error. If no recovery occurs proceed to step 2.
2. Restore to track 0.
3. Repeat the operation in error.
4. Repeat steps 2 and 3 three times in anticipation of error recovery.
5. If the error persists beyond this sequence, it should be considered irrecoverable.

A modification of this sequence may, of course, be more suitable for a specific operation.

4.3 BOOTSTRAPPING FROM THE MODEL 1950

Two methods are available to bootstrap the computer from the Model 1950. Both methods allow the user to move one bootstrap block (Block 0) from the Model 1950 to memory and begin execution of the data in this block.

The bootstrap when executed moves one sector (block) of data from Block 0 (sector 0 of track 0 of unit 0) of the Model 1950 to memory locations 0 through (sector size-2) of memory field 0. When the transfer is complete a jump to location 0 occurs and program execution begins at that location. Therefore the bootstrap block must be written on Block 0 in such a way that the first executable instruction will be read into location 2 (the second word of the block).

4.3.1 Hardware Bootstrap

A ROM board is available from ESI which allows the user to internally bootstrap the system. To use it, the user should:

1. Halt the computer
2. Load address 167716
3. Start

4.3.2 Software Bootstrap

The following code can be loaded in memory at location 1000 or greater. Location 1000 is shown as an example.

Address	Code
1000	5037
1002	167204
1004	5037
1006	167200
1010	32737
1012	4000
1014	167200
1016	1374
1020	5007

Begin execution at location 1000.

```
1                       ;
2                       ;
3                       ; PROGRAMMING EXAMPLE
4                       ;
5                       ; THIS PROGRAM COPIES EACH SECTOR OF THE DISK
6                       ; IN UNIT 0 TO THE CORRESPONDING SECTOR OF UNIT 1.
7                       ; TRANSFER IS DONE WITHOUT INTERRUPTS, AND A FULL
8                       ; SECTOR TRANSFER IS DONE IN EACH CASE.
9                       ; EIGHT SECTOR FORMAT IS ASSUMED, THUS 1000 (OCT)
10                      ; TRANSFERS ARE COMPLETED.
11                      ;
12                      ;
13      000000                  .ASECT
14      000600                  .=600
15                      ;
16                      ; DISK REGISTERS
17                      ;
18 00600 167204 XFDDA:  167204          ;DISK ADDRESS REGISTER
19 00602 167202 XFDMA:  167202          ;MEMORY ADDRESS REGISTER
20 00604 167200 XFDCM:  167200          ;COMMAND REGISTER
21 00606 167200 XFDST:  167200          ;STATUS REGISTER
22                      ;
23                      ; REGISTER ASSIGNMENTS
24                      ;
25      000000 R0 = %0
26      000001 R1 = %1
27      000002 R2 = %2
28      000005 R5 = %5
29                      ;
30                      ;
31                      ;
32                      ;
33 00610 005001 INIT:   CLR     R1              ;T/S ADDRESS
34 00612 012702         MOV     #BUF,R2         ;BUFFER ADDRESS
         000752
35 00616 004567 RESTOR: JSR     R5,DRIVER       ;RESTORE UNIT 0
         000046
36 00622 000103         .WORD   0103            ;UNIT # AND COMMAND
37 00624 000774         BR      RESTOR          ;ERROR RETURN
38 00626 004567         JSR     R5,DRIVER       ;RESTORE UNIT 1
         000036
39 00632 002103         .WORD   2103            ;UNIT # AND COMMAND
40 00634 000770         BR      RESTOR          ;ERROR RETURN
41 00636 004567 LOOP:   JSR     R5,DRIVER       ;READ A SECTOR
         000026
42 00642 000000         .WORD   0               ;UNIT # AND COMMAND
43 00644 000764         BR      RESTOR          ;ERROR RETURN
44 00646 004567         JSR     R5,DRIVER       ;WRITE ON UNIT 1
         000016
45 00652 002001         .WORD   2001            ;UNIT # AND COMMAND
46 00654 000760         BR      RESTOR          ;ERROR RETURN
47 00656 005201         INC     R1              ;INCREMENT T/S ADDRESS
48 00660 022701         CMP     #1000,R1        ;DONE?
         001000
49 00664 002764         BGT     LOOP            ;NOPE - TRANSFER NEXT
50 00666 000000         HALT                    ;YES.  HALT.
```

Figure 4-1. Programming Example

```
.MAIN.  MACRO VR05A 01-JAN-72 00:00 PAGE 2


                        ;
                        ;
                        ; DRIVER SECTION
                        ;
                        ; T/S ADDRESS IN R1 AT ENTRY
                        ; BUFFER ADDRESS IN R2 AT ENTRY
                        ;
                        ; CALL: JSR  R5,DRIVER
                        ;       I/O COMMAND (BITS 0-7), UNIT # (BITS 10:11)
                        ;
                        ;
000670 011500 DRIVER: MOV     (R5),R0           ;GET UNIT # & COMMAND
000672 042700         BIC     #171777,R0        ;MASK TO UNIT ONLY
       171777
000676 060100         ADD     R1,R0             ;UNIT # + T/S ADDRESS
000700 010077         MOV     R0,@XFDDA         ;SEND DISK ADDRESS
       177674
000704 010277         MOV     R2,@XFDMA         ;SEND MEMORY ADDRESS
       177672
000710 012500         MOV     (R5)+,R0          ;GET COMMAND
000712 042700         BIC     #177400,R0        ;CLEAR ALL BUT COMMAND
       177400
000716 010077         MOV     R0,@XFDCM         ;SEND COMMAND
       177662
000722 017700 BUSY:   MOV     @XFDST,R0         ;GET STATUS
       177660
000726 032700         BIT     #14000,R0         ;BUSY?
       014000
000732 001373         BNE     BUSY              ;YES
000734 017700         MOV     @XFDST,R0         ;NO - GET STATUS
       177646
000740 100402         BMI     ERROR             ;ERROR.
000742 005725         TST     (R5)+             ;INCREMENT RETURN
000744 000205         RTS     R5                ;RETURN #2 - NO ERROR
000746 000000 ERROR:  HALT                      ;HALT
000750 000205         RTS     R5                ;RETURN #1 - ERROR
                        ;
                        ; BUFFER
                        ;
000752 000752 BUF:    .=.
       001752 BUFL = BUF+1000          ;256 WORD BUFFER
                        ;
                        ;
       000001'          .END

.MAIN.  MACRO VR05A 01-JAN-72 00:00 PAGE 2+
SYMBOL TABLE

BUF     000752          BUFL  = 001752          BUSY    000722
DRIVER  000670          ERROR   000746          INIT    000610
LOOP    000636          RESTOR  000616          R0    =%000000
R1    =%000001          R2    =%000002          R5    =%000005
XFDCM   000604          XFDDA   000600          XFDMA   000602
XFDST   000606
. ABS.  000752     000
        000000     001

ERRORS DETECTED:  0
FREE CORE:  5463. WORDS
PP:,KB:<DRIVER.PAL
```

Figure 4-1. Programming Example (Continued)

4.4 FLEXIBLE DISK DIAGNOSTIC PROGRAMS

4.4.1 Program Description

The disk diagnostic program enables the user to 1) exercise all positioning and data transfer functions provided by the formatter, 2) check all status and error flags returned by the formatter, 3) verify proper operation of all units connected to the formatter and, 4) verify that part of the computer interrupt system used by the formatter. Some of the tests included in the diagnostic are designed to isolate errors which depend on the data content or length of a data transfer. Another set of tests are devoted to forcing error conditions and checking that they are properly reported by the controller. Tests are also provided to check for proper sector formatting and unit to unit compatibility.

Error reporting is accomplished via the terminal. In general, errors are reported when either status information or data input from the controller differ from that expected by the program. The operator has the ability to inhibit error message outputs as required. In addition, the operator specifies the order in which tests are performed and the sequence in which certain tests select units.

4.4.2 Operating Instructions

The diagnostic executes in a sequence of well defined steps that are described below. All communications between the operator and the program are via the terminal. All replies to specific input requests are entered from the keyboard and are terminated by the RETURN key. The program ignores any characters other than the 64 printing characters (including space) RUBOUT, RETURN, and the "break" characters Control-U, Control-E, Control-T, Control-N, and Control-F.

The RUBOUT character is an input line-editing character and may be used by the operator to correct errors made while typing. Its function is as follows:

RUBOUT — Deletes one character to the left for each input and echoes back as /.

The break characters are used to alter the execution sequence of the diagnostic as follows:

Control-F — Returns program to the FMPR request (step 3 below), and echoes back as ↑F.

Control-U — Returns program to the UNIT request (step 4 below), and echoes back as ↑U.

Control-E Returns the program to the EMSK request (step 5 below), and echoes back as ↑E.

Control-T Returns the program to the TEST request (step 6 below), and echoes back as ↑T.

Control-N Stops execution of the test in progress, starts execution of the next test in the sequence specified by the last TEST request, and echoes back as ↑N.

Not all of the break characters are recognized at each step in the program's execution sequence, therefore, those break characters that are recognized are specifically indicated in the steps described below.

All numeric values input to or output from the program, unless otherwise specified, are in octal. If more than 6 digits are input for a numeric value, then the program will recognize only the low ordered 16 binary bits of the value specified.

If any operator reply to an input request cannot be recognized by the program or is outside of the allowed set of values, then the program will output the error message:

???

and repeat the request. Similarly, for input requests in which the operator may input a variable number of parameters, the program will output the error message:

TOO MANY

and repeat the request if the number of parameters exceeds the maximum allowed.

1. Load the disk diagnostic program into the computer. (The program is called "DIAG" when loaded directly from the floppy disk.) Once loaded, the program will automatically start execution as indicated in step 2, below. (The program can be manually restarted at location 600_8.)

2. The program now types out the size and locations of the I/O buffers as:

   WBUF = a
   RBUF = b
   BUFL = c
   ENCM = d

Where a is the starting address of the write buffer, b is the starting address of the read buffer, c is the buffer length, and d is the last memory location used by the program.

Following this step the program enters its normal execution sequence.

Example:

```
WBUF = 14266
RUBF = 15366
BUFL =   414
ENDM = 77376
```

The test has just been loaded, the write buffer starts at 14266_8, the read buffer at 15366_8, the length of each buffer is 414_8 words (1030_8 bytes), and the last word of core used is 77376_8.

3. The program requests information describing the disk formatter configuration by typing:

   FMPR =

   The operator replies by entering 4 numbers in the sequence w, s, d, i, separated by commas. These numbers describe:

   w = Number of words per sector
   s = Number of sectors per track
   d = Device address of the coupler status register
   i = Interrupt vector address of the coupler

   Legitimate combinations are shown in the table below:*

Words Per Sector (Decimal)	n	s	d	i
256	400	10	3	i
128	200	20	d	i

   The w, s numbers must be entered or an error message will be printed. The d, i specifications may be defaulted by typing a carriage after the number of sectors per track ("s") is entered. In this case, the program assumes:

   d = 167200
   i =   374

*Typical entry for ESI systems is 400,10,,140

4. The program request the identity and sequence of the disks to be tested by typing:

   UNIT =

   The operator replies by entering numbers in the sequence:

   *UNIT = U_1, U_2, --- U_n

   where Ui = $UT_1 - T_2$ or U/T

   in the first case: Ui = $UT_1 - T_2$

   u = Unit number of disk drive
   T1 = Lower track number to be tested
   T2 = Upper track number to be tested

   in the second case: Ui = U/T

   u = Unit number of disk drive
   O = Lower track number to be tested (default)
   T = Upper track number to be tested

   Being able to specify $T_1 - T_2$ enables the user to run diagnostics on his disk only on the tracks specified allowing him to protect data on the remainder of the disk.

   The program recognizes the break character Control-U during this step.

5. The program requests the masks used to control error message printing by typing:

   *EMSK =

   The operator replies by entering up to three numbers in the form:

   m, n

   which describe one error word mask and a detail line limit.

   The error word mask is examined by the program when a discrepancy occurs between the expected outcome and the actual outcome of any operation performed by the diagnostic tests. If the mask bit corresponding to a particular discrepancy is set, then the program outputs an error message. Otherwise, the message is inhibited.

   The bits assigned to the error word and thus m are shown in Table 5.

*Typical entry for ESI systems is Ø/77 or 1/77.

Bit	Value	Interpretation
7	200	Not Ready
6	100	Time-Out Error
5	40	Write Protect Error
4	20	Format Error
3	10	Rate Error
2	4	Preamble Compare Error
1	2	CRC Error
0	1	Seek

Table 4-1.

If m is omitted, a mask of 377 is assumed.

"m" is a number that specifies the maximum number of detail lines to be printed following a verify error message. If specified as 0, no detail lines will be outputted; if omitted, all detail lines will be outputted.

The program recognizes the break characters Control-U and Control-E during this step.

Example:

*EMSK = 0040, 3
Sets error print mask to 0040 (WPR error only), and the verify detail line limit to 3.

6. The program requests the tests to be performed by typing:

TEST =

The operator replies by entering from 1 to 24 test specifications separated by commas. Each test specification consists of either a single number or two numbers separated by a dash (-). The first form specifies a single test and must be from the following list:

TEST

0 Check Read Sectors
1 Format Sectors
2 Verify Sector Addresses
3 Seek and Restore
4 Write 1/2 Sector
5 Read 1/2 Sector
6 CRC Generation
7 Memory Addressing
10 Data Patterns
11 Random Parameters

*Typical entry for ESI system is a carriage return.

12 CRC Compare Error
13 Interrupt Functions
14 Timeout Error
15 Rate Error
16 Write Protect Check
17 Not Ready

The second form, n_1 - n_2, specifies a range of tests with both n_1 and n_2 selected from the values given above and, n_1 less than n_2. The operator may, in addition, request that a given specification be used repeatedly by preceding the specification with 'n*' where n is the number of times the test (or tests) is (are) to be repeated.

n must be in the range $0\text{-}7777_8$. If n = 0 is given, then the specified test(s) will be repeated indefinitely. If no test specifications are input, or if a specification is omitted, then the program will assume a test specification of:

1-14

The program recognizes the break characters Control-U, Control-E, and Control-T during this step.

Example:

Test=5,3*11,2*2-4,0*6
Specifies the test sequence 5, 11, 11, 11, 2, 3, 4, 2, 3, 4, and 6 repeated indefinitely.

7. The program proceeds to execute the tests specified in Step 6 on the UNITs specified in Step 4. When the specified test sequence has completed the program will return to Step 6.

   The program recognizes all of the allowed break characters during this step.

4.4.3 Error Messages

The printing of error messages is completely controlled by the status mask specified by the operator. Three types of error messages are output by the program, one as a result of status errors returned by the formatter (hardware errors), one resulting from errors in the data input from the formatter (verify errors), and the last resulting from errors in the functioning of the status register or interrupt system. The printing of hardware error messages is controlled by bits 0-16 of the error mask, and correspond to actual bits returned in the formatter status register. Further description of the meaning and interpretation of information input from the status, error, and sector address registers can be found in the Model 1950 I/O Specification section.

Following each operation performed by the diagnostic, the contents of the status register are compared with the status that the program expects to receive at that point. If one or more bits in the register is other than expected and if the corresponding bit is set in the status mask word then a hardware error message is printed.

Hardware error messages have the format:

```
H dddd     OP=oooo,wwwww     AD=u, tt, ss     ST=eeeeee,rrrrrr
```

and are interpreted as follows:

H dddd	dddd is the current test state of the test in progress.
OP=oooo,wwwww	oooo is the disk operation being performed (see I/O Specification), and wwwww the word count output to the disk formatter when the operation began. (The buffer address is WBUF for write operations and RBUF for read operations).
AD=u, tt, ss	u is the disk unit number (0-3), tt is the track number, ss is the sector number.
ST=eeeeee,rrrrrr	eeeeee is the expected value and rrrrrr the received value of the formatter status register.

The printing of verify error messages is controlled by the detail line limit. Verify error messages occur when data read in from the controller differs from that which is expected by the program. Each verify error message consists of one line to notify the operator that a verify error occurred followed by a detail line for each data word in error.

The format of these messages is:

```
V dddd      OP=oooo,wwwww      AD=u, tt, ss      EC=nnnn
  aaaa          eeeeee             rrrrrr
   :             :                  :
```

and is interpreted as follows:

V dddd	dddd is the current test state of the test in progress.
OP=oooo,wwwww	oooo is the disk command and wwwww is the word count output to the disk formatter during the last operation. (The buffer address is RBUF.)
AD=u, tt, ss	u is the disk unit number (0-3), tt is the track number, ss is the sector number.
EC=nnnn	nnnn is the number of data words in error (i.e., the number of detail lines to follow).

aaaa is the address, relative to WBUF and RBUF, of the data word in error.

eeeeee is the expected data word, and

rrrrrr is the received data word.

The number of detail lines printed will be the minimum of the detail line limit and the error count. In addition, the operator may, while the detail lines are printing, delete the printing of the remaining detail lines associated with the verify message by entering any key from the terminal keyboard. In this case, the program will output * and continue with the test in progress.

The printing of interrupt errors can occur during Test 13.

The format is: IA=aaaa where aaaa indicates the test state.

4.4.4 Test Descriptions

NOTES ON THE USE OF THE DIAGNOSTIC

NOTE Ø: In the test descriptions which follow, MNTK refers to the smallest track address selected by the user and MXTK refers to the largest track address selected. For example, if the user responds:

UNIT = Ø/5-3Ø

then MNTK=5, MXTK=3Ø. WPSC refers to the number of words per sector.

NOTE 1: FORMATTING A PACK: When running the diagnostic with an unformatted pack, Test 1 may be used to properly format the pack. Thus it is a prerequisite to tests Ø, 2-16. See the description of Test 1 for further details.

NOTE 2: DATA PATTERNS: The data patterns used in the various tests are as follows:

PATTERN Ø: All bits are reset in all words:

Ø, Ø, Ø, ...

PATTERN 1: All bits are set in all words:

177777, 177777, 177777, ...

PATTERN 2: Bits alternate:

Ø52525, Ø52525, Ø52525, ...

PATTERN 3: Increasing count (resetting after each full sector of data)

FIRST SECTOR: 0 1, 2, 3, 4, ...
NEXT SECTOR: 0 1, 2, 3, 4, ...

PATTERN 4: Pseudo-random data

PATTERN 5: A one bit in a zero bit environment

FIRST TIME: 1, 1, 1, ...
SECOND TIME: 2, 2, 2, ...
THIRD TIME: 4, 4, 4, ...

⋮

SIXTEENTH TIME: 100000, 100000, 100000, ...

PATTERN 6: A zero bit in a ones environment

FIRST TIME: 177776, 177776, 177776, ...
SECOND TIME: 177775, 177775, 177775, ...
THIRD TIME: 177773, 177773, 177773, ...

⋮

SIXTEENTH TIME: 077777, 077777, 077777, ...

PATTERN 7: An increasing byte count

0001, 001003, 002005, 003007, ...
(In terms of bytes: 0, 1, 2, 3, 4, 5, 6, 7, ...)

4.4.4.1 Test 0: Check all Sectors

PURPOSE: To determine whether all sectors on the tracks selected by the user are properly formatted.

PREREQUISITES: Test 1

STATES: 0

TEST PROCEDURE: A check read is performed on all sectors of all tracks defined by UNITS specifiers. Hardware errors may occur and the nature of the error may be determined from the error printout. For example, an error printout as follows:

H 0000 OP=0000,00400 AD=0, 01, 7 ST=000000, 000004

would indicate that sector 7 of track 1, unit 0 has an incorrect preamble.

If a preamble check error occurs on a given track, Test 1 should be re-run on that track, then Test 0 repeated. If the error persists, Test 2 may be run to determine exactly what preamble exists on the sector in question.

4.4.4.2 Test 1: Format all Sectors

PURPOSE: To format a new disk or prepare a disk for a series of diagnostic tests. Test 1 is normally the first test to be run in the diagnostic sequence.

PREREQUISITES: None

STATES: 0

TEST PROCEDURE: This test writes a correct preamble, known data field, and correct CRC for each sector of each track of each unit as defined by UNITS. The data field contains the unit number in word one, the track number in word two, and the sector number in word three. The remainder of the data field contains all zeroes. The CRC and preamble are generated by the formatter.

ERRORS: Hardware errors reported may imply a drive error (NRDY, BUS ERR) or an improper selection of a parameter by the user (RE).

4.4.4.3 Test 2: Verify all Sector Addresses

PURPOSE: To test the sector-addressing logic of the formatter.

PREREQUISITES: Test 1

STATES: 0

TEST PROCEDURE: The data which was written on each sector in Test 1 is read and verified.

ERRORS: If Test 2 reports verify errors, the 3 words will identify the sector which was actually read to check whether the sector-adddressing logic is functioning properly. For example, the following error:

```
V0000  OP=0000, 0400  AD=0, 04, 05  EC=0001
000002 000005 000032
```

would most likely indicate that wrong sector on the given track was being addressed. Or this printout;

```
V0000  OP=0000,0400  AD=0, 07, 00  EC=00001
00001 000007 000003
```

would indicate that the wrong track was being addressed.

4.4.4.4 Test 3: Seek and Restore

PURPOSE: To check the seeking and restoring function of each drive selected.

PREREQUISITES: Test 1

STATES: 0, 1

TEST PROCEDURE: STATE 0: Using a random pattern of track addresses, 100 tracks are check read, seeking from the current head position to the next random track address. (Only tracks within the user-defined limits of UNITS are checked.)
STATE 1: Using a random pattern of track addresses, 100 tracks are check read with the restore bit set, thereby seeking to track 0 before seeking the next track. (Only tracks within the user-defined limits of UNITS are checked.)

ERRORS: A Preamble Compare Error probably indicates the positioning logic (including servos, etc., in the drive) is failing.

4.4.4.5 Test 4: Write Half Sector

PURPOSE: To test the half-sector write logic.

PREREQUISITES: Test 1

STATES: 0, 1

TEST PROCEDURE: STATE 0: One-half sector of data (pattern 1) is written. (The formatter fills the remainder of the

sector with zeroes.) The full sector of data is then read and a check is made to verify that exactly 1/2 sector of ones and 1/2 sector of zeroes was read.

STATE 1: A full sector of data (pattern 1) is written, read, and verified to see that 1/2 sector mode can be cleared.

ERRORS: A verify error may indicate failure to divide the sector correctly. Note that the expected data is always 000000 or 177777. If one of these numbers appears when the other is expected it is symptomatic of the above. Any other data pattern (e.g. 177577) probably indicates an ordinary data error. A verify error not preceded by a hardware error (CRC) also may indicate the sector-splitting logic has failed.

4.4.4.6 Test 5: Read Half Sector

PURPOSE: To test the half-sector read logic.

PREREQUISITES: Test 1

STATES: 0

TEST PROCEDURE: A full sector of data (pattern 1) is written on a sector with a standard write command. The read buffer is zeroed and 1/2 sector of data is read. Correct input into the first half of the buffer and integrity of the second half are then verified.

ERRORS: Same as Test 4.

4.4.4.7 Test 6: CRC Generation

PURPOSE: To test the CRC generating and CRC checking logic in the formatter.

PREREQUISITES: Test 1

STATES: 000, 100, 200, 300, 400

TEST PROCEDURE: The states differ only in which data pattern is being used, (patterns 0, 1, 2, 3 and 4 are generated for this test) and which iteration of that pattern is currently occuring.

For each pattern, one sector of data is written, the correct CRC for that data is calculated by the software, and the sector of data plus its CRC is read and verified.

Next, a sector of data and its correct CRC is written and a normal read is performed verifying no CRC error occurs.

ERRORS: Suppose WPSC=400

```
V0200 OP=0001,0400 AD=0,77,00 EC=00002
000400  137536  007010
```

would indicate that the CRC words are not being properly generated.

```
H 0200  OP=0000,0400  AD=0,77,00  ST=000000,000001
```

would indicate that the CRC checking logic was at fault.

4.4.4.8 Test 7: Memory Addressing

PURPOSE: To check the operation of the memory address register in the coupler.

PREREQUISITES: Test 1

STATES: 0, 1

TEST PROCEDURE: The memory-addressing function of the coupler is tested both on a read and a write by generating a data pattern in the end of core so that the contents of word m is m itself (masked to the number of bits in a computer word). The end of core is then split up into buffers, each buffer being the same size as one sector.
STATE 0: Data is written from each buffer in memory, read back to a fixed buffer and verified.
STATE 1: Data is written from a fixed buffer and read back to each buffer in memory to be verified.

ERRORS: For example:

```
V0000  OP=0000,0400  AD=0,77,00  EC=0400
00000  047026  007026
00001  047030  007030
00002  047032  007032
```

would indicate that the coupler was not addressing memory address 47026 correctly on a write operation.

4.4.4.9 Test 10: Data Patterns

PURPOSE: To test the fidelity of data transfer using various data patterns and writing on certain selected tracks on the disk. This test also prepares the disk for Test 11.

PREREQUISITES: Test 1

STATES: 0, 1, 2, 3, 4, 5, 6, 7777

TEST PROCEDURE: STATE 0: Pattern 0 is written onto one full sector from each track within the limits of UNITS. The data is then read back from each sector to verify the data transfer.
STATE 1: Pattern 1 is used rather than pattern 0.
STATE 2: Pattern 2 is used.
STATE 3: Pattern 3 is used.
STATE 4: Pattern 4 is used.
STATE 5: Pattern 5 is used.
STATE 6: Pattern 6 is used.
STATE 7777: At each sector on all tracks selected by the user, one full sector is written consisting of four sector-identifying words followed by WPSC-4 words of data pattern 7 (incrementing bytes). This prepares the disk for Test 11.

4.4.4.10 Test 11: Random Parameters

PURPOSE: To test that the formatter can accurately address all parts of each disk accurately, and read data accurately from all the units it is controlling.

PREREQUISITES: Test 1, Test 10

STATES: 0

TEST PROCEDURE: This test is in the nature of an exerciser. A unit number, track number, and sector number are all randomly selected, a read is performed and the data generated by Test 10 (state 7777) is verified.

ERROR MESSAGES: Multiple errors on a sector, especially in the absence of a hardware error message, may indicate failure of the track select, unit select, or rotational position logic.

4.4.4.11 Test 12: CRC Compare Error

PURPOSE: To test the logic associated with the CRCE bit in the status word and the CRC checking logic.

PREREQUISITES: Test 1

STATES: Ø, 1ØØ, 2ØØ, 3ØØ, 4nn (where nn = Ø-12)

TEST PROCEDURE: Using several data patterns the program writes a sector in diagnostic mode, complementing in turn each of the 16 bits of the CRC word. After each write operation the sector is read twice with a normal read operation and the CRC error status bit is checked for a positive state. After the 16th bit for the fifth data pattern has been tested, the sector is re-written with a normal write command.

ERRORS: If the disk status fails to report a CRC error, an error message will be printed.

4.4.4.12 Test 13: Interrupt System

PURPOSE: To test that the formatter returns BUSY and DONE to the CPU correctly and that the CPU responds correctly according to whether interrupts are enabled or disabled.

PREREQUISITES: None

STATES: Ø, 1, 2, 3

TEST PROCEDURE: STATE Ø: In state Ø a seek only to MXTK is peformed with interrupts disabled. It is verified that no interrupt occurred.
STATE 1: A read (operation 3) is performed on MXTK with interrupts disabled. It is verified that no interrupts occurred.
STATE 2: A seek only to MXTK is performed with interrupts enabled. It is verified that no interrupt occurred, as a seek command should not generate an interrupt.

STATE 3: A read is performed on MXTK with interrupts enabled; it is verified that an interrupt did occur.

If during this test an interrupt occurs when it should not, or one does not occur when it should an error message of the form IA=n is typed out where n=TEST STATE.

4.4.4.13 Test 14: Time-Out Error

PURPOSE: To check that various conditions will cause the time-out error bit to be set in the status word.

PREREQUISITES: TEST 1

STATES: Ø

TEST PROCEDURE: An attempt is made to address a non-existent track and sector. It is expected that the time-out error bit will be set in the status word.

NOTE: This test should not be specified for formatters with 16 sectors per track.

4.4.4.14 Test 15: Rate Error

PURPOSE: To test that various conditions will cause the Rate Error bit to be set in the status word.

PREPREQUISITES: None

STATES: Ø

TEST PROCEDURE: A read operation is initiated, then a HALT instruction is issued. After CONT is pressed, status is checked to verify a rate error occurred.

OPERATOR ACTION: Press CONT after the HALT.

4.4.4.15 Test 16: Write Protect Flag Error

PURPOSE: To test the logic associated with the write protect bit in the status word.

PREREQUISITES: Test 1

STATES: Ø

TEST PROCEDURE: A write is attempted on a protected pack, looking for a write-protect error in the status.

OPERATOR ACTION: The computer will HALT after printing "Test 16". The operator should insert a write-protected disk in the first selected unit and press CONT when the unit is up to speed. On the second HALT, remove the write-protected disk, wait for the unit to return to speed, and press CONT again.

4.4.4.16 Test 17: Not Ready

PURPOSE: To check the operation of the Not-Ready bit in the status word.

PREREQUISITES: None

STATES: Ø

TEST PROCEDURE: For the first unit defined in UNITS, an attempt is made to select that unit while it is OFF-LINE.

OPERATOR ACTION: When the computer HALTs, place the unit in an OFF-LINE state (turning power off or opening the door) and press CONT. Return the unit to an ON-LINE state at any time thereafter.

4.5 MNEMONICS AND OPERATIONS SUMMARY

BBSY - Bus Busy
BGI - Bus Grant In
BR - Bus Request
BUS ERR - Bus Error
BWTC - Bit Word Time Clock
CCE - Cyclic Check Error
COSP - Coupled Output Strobe Pulse
CRC - Cyclic Redundancy Check or Check Character
CRCI - CRC Input
CREQ - Clear Request
CRCE - CRC Error or Check Character Compare Error
DATA - Data
DIN - Data In
DOUT - Data Out
DSECTOR - Data Sector
DSTRB - Data Strobe
DSTROBE - Data Strobe

DWD	-	Data Word
DWREN	-	Drive Write Enable
ENCCG	-	Enable Cyclic Code Generator
ENSLC	-	Enable Select
FE	-	Format Error or Fatal Error
FLAG	-	Flag
GID	-	Gated Input Decode
GMAD	-	Memory Address Gate
GOD	-	Gated Output Decode
GPRE	-	Preamble Gate
HSI	-	Half Sector Inhibit
IFLG	-	Interrupt Flag
IMSYN	-	Internal Master Sync.
INC	-	Increment
INTEN	-	Interrupt Enable
ISP	-	Input Strobe Pulse
LDCM	-	Load Command Word
LDCMD	-	Load Command
LDDA	-	Load Disk Address
LDHD	-	Load Head
LDMA	-	Load Memory Address
LSLCTC	-	Load Select Time Clock
ME	-	Memory Extension
MCLR	-	Master Clear
MSTR	-	Master Strobe
NPG	-	Non-Processor Grant
NPR	-	Non-Processor Request
NRDY	-	Not Ready
OSP	-	Output Strobe Pulse
PCE	-	Preamble Compare Error
PRE	-	Preamble
PRED	-	Preamble Delay
RD	-	Read Data
RATE	-	Rate Error
RE	-	Rate Error
RDST	-	Read Disk Status
RDMA	-	Read Memory Address
RDY	-	Ready
REGSEL	-	Register Select
SACK	-	Slave Acknowledge
SC	-	Sector Compare
SCLK	-	Shift Clock
SDATA	-	Serial Data
SEEKING	-	Unit Seeking
SLC	-	Select
SP	-	Sector Pulse
SSYN	-	Slave Sync.
STRB	-	Strobe
TA	-	Track Address
TOE	-	Time Out Error
WE	-	Write Error
WPE	-	Write Protect Error

SECTION 5
TECHNICAL DESCRIPTION

5.1 GENERAL

Figure 5-1 illustrates the overall 1950 block diagram. These blocks are directly related to their functional components (i.e., boards).

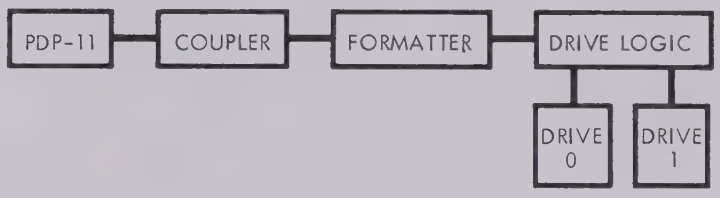


Figure 5-1. 1950 Block Diagram

The Coupler provides the interfacing between the PDP-11 and the floppy disk electronics. It provides the NPR and BR interrupt logic, address decoding and data buffering.

The Formatter controls the data transfer timing, data formatting and error detection. It decodes the commands from the Coupler to select the correct drive and initiates actions.

The Drive Logic provides the hardware interface between the Disk Drives and the Formatter and is primarily concerned with signal steering and head control.

5.2 COUPLER

NOTE: Refer to the "PDP-11 Peripherals Handbook" for an understanding of the computer handshake sequence.

The PDP-11 Coupler Board (P/N 42559) block diagram is shown in Figure 5-2. The numbers shown in parenthesis refer to schematic sheet numbers containing the location of functional blocks.

The floppy address from the computer is buffered by IC's A3 and C5 on (1) and A4, A5 and A6 on (2). Buffered address lines are decoded in B7 and B8 on (1) to form the base address of 16720X. Notice that this base address can be modified using the jumpers near B7 and B8.

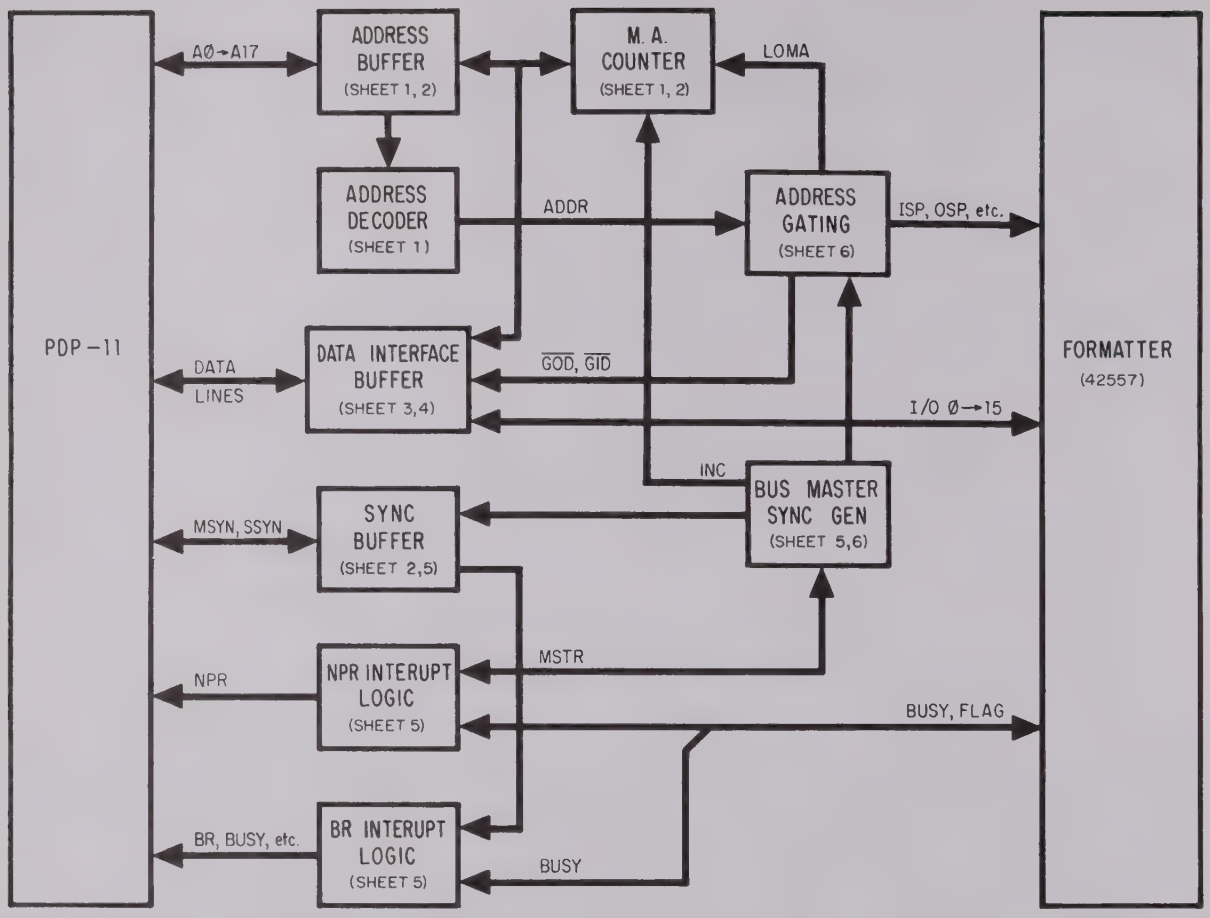


Figure 5-2. Coupler Block Diagram

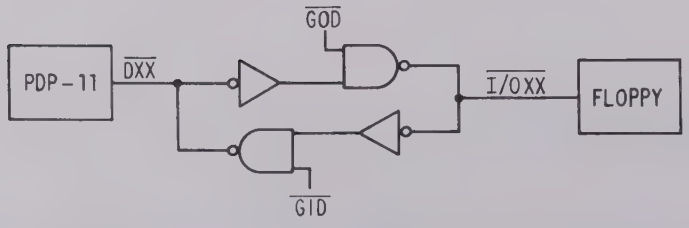


Figure 5-3. Data Transmission Path

The base address is synchronized by the computer MSYN in gate E3 on (6) to form a synchronizing strobe for all address gating. Notice that the base address drives gates F5, E6 and E7 which eventually form floppy strobe signals $\overline{\text{REG SEL}}$, $\overline{\text{ISP}}$ and $\overline{\text{OSP}}$.

The data interface buffers for the 16 I/O bits are shown on Schematics 3 and 4. A typical data bit transmission path is shown in Figure 5-3.

Data is strobed to and from the computer by $\overline{\text{GID}}$ and $\overline{\text{GOD}}$ respectively (6).

Data transfers between the computer and the floppy are controlled by the interrupt circuits shown in Schematic 5. The upper half of Schematic 5 contains the NPR circuits and the lower half the BR circuits. All word transfers use the NPR section. The lower (BR) section is only used to indicate the completion of a block transfer.

During a normal transfer action, a load command word (LDCM) at address 167200 initiates the transfer by setting the busy flip-flop (7) of the Formatter. This busy signal enables flip-flop E2 (6) in the Coupler. The Formatter also sends a flag clock indicating a word is ready for transfer. E2 is set by this action which generates an NPR to the computer.

When the computer responds, state counters D2 and D3 (6, upper half) go to the "11" state which initiates $\overline{\text{MSTR}}$ at the output of C8-8. A handshake occurs between the Coupler and the computer which generates IMSYN and SSYN; eventually triggering one shot F4 (6) to form $\overline{\text{INC}}$. $\overline{\text{INC}}$ clocks the memory address counters B4 and B5 (2) and B3 and C6 (1) so that the next transfer will have the correct address. Figure 5-4 illustrates a typical transfer.

The above sequence occurs for each word transferred in a given block. This results in 256 NPR requests per full block. Figure 5-5 illustrates a typical block transfer.

At the conclusion of the block transfer, Busy is reset clocking flip-flop E2 (5) if the interrupt has been enabled. The output of E2 generates a BR which begins a BR interrupt sequence with a vector of 140. State counters D2 and D3 (5, lower half) control this sequence. If other blocks are to be transferred, the computer will then initiate another NPR sequence.

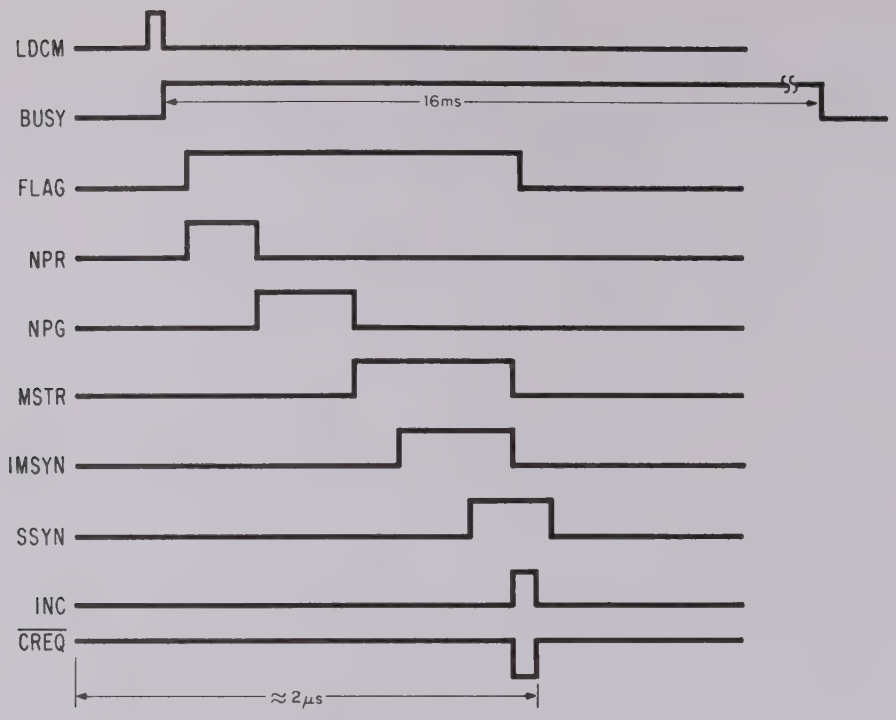


Figure 5-4. Typical Word Transfer

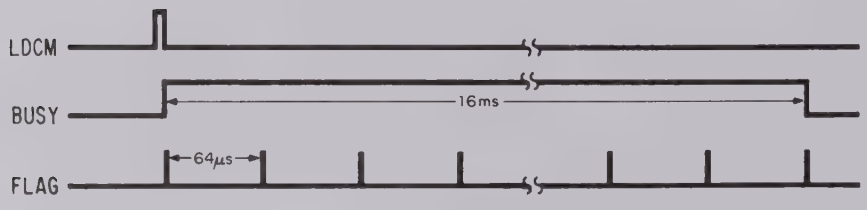


Figure 5-5. Typical Block Transfer

5.3 FORMATTER

The floppy Formatter (P/N 42557) block diagram is shown in Figure 5-6.

The data I/O buffers (1 and 2) transfer the 16 data bits between the Coupler and the Formatter. Data read from the disk is shifted into shift registers C7 and D4 (1) and on into E6 and E4 (2). Their outputs pass through storage multiplexers B7, C4, D6 and E5 where they are stored while the next word is shifted into the shift register. The data then continues through multiplexers D7 and D5 for the lower order bits and on through transceivers A7, A5, B6 and B5 to the Coupler.

Data to be loaded into the disk reverses the above procedure. After data is loaded into the shift registers, it is shifted out to the disk from E4 (2) at signal SR15 and passes through K1, L4 and A1 (4). During a normal write cycle, L4 (4) multiplexes the information to be recorded in the format shown in Figure 2-3.

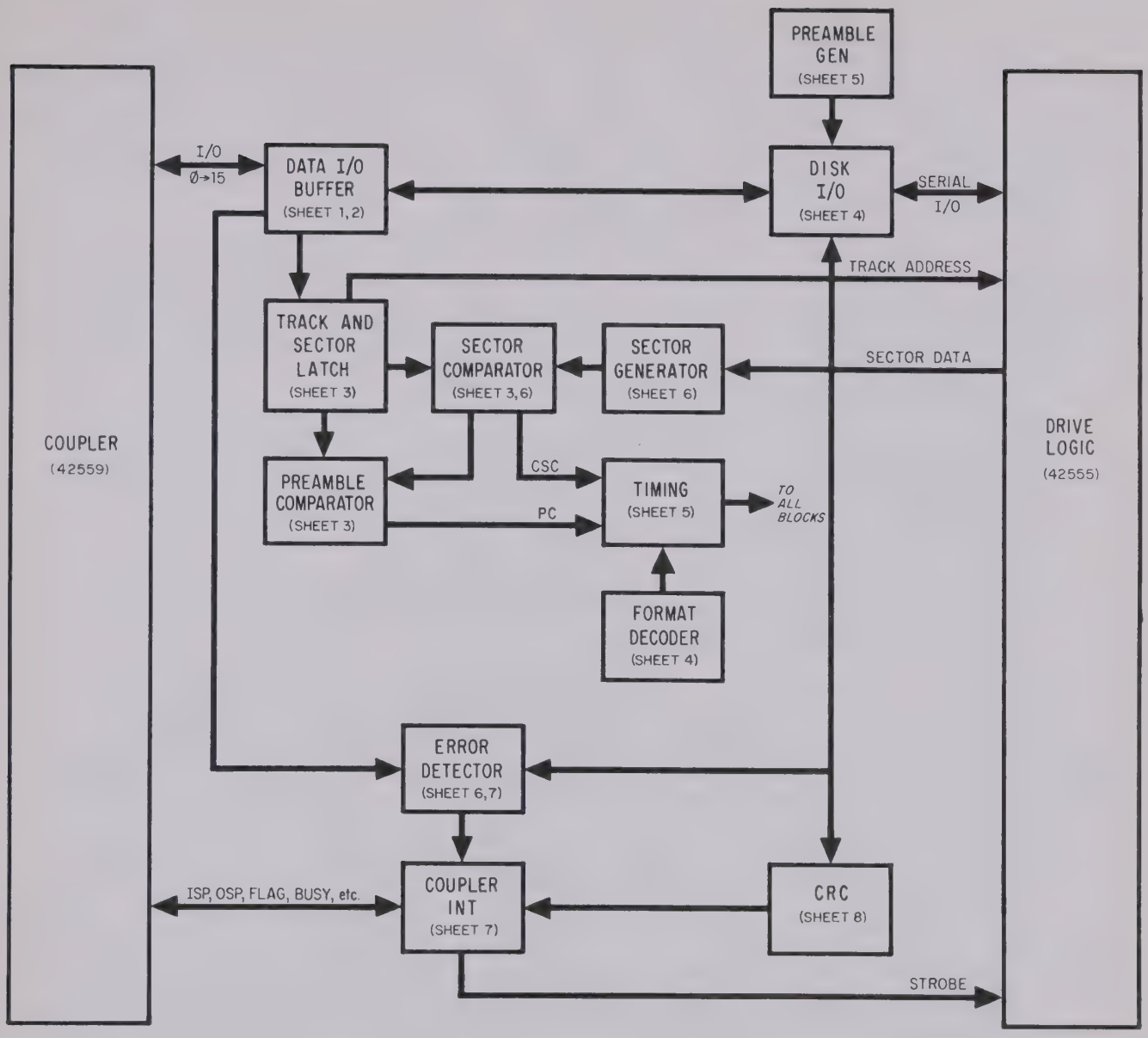


Figure 5-6. Formatter Block Diagram

After the field of 128 zeroes is recorded, L4 selects the "PRE" signal at L4-5, which originates from the preamble generator (5). This signal consists of data selectors E2 and F2 and gates G1 and F1. The signal form is shown in Figure 2-4. L4 (4) then selects the serial data via K1 followed by the CRC word from M4 (8).

The track and sector latch consists of E3 and F4 (3). Here the track and sector preamble recorded on the disk is stored after it is read in. It is then checked against the desired track and sector in comparators F7, P3 and F5 (3). The output, at F5-6, forms the preamble compare signal "PC" which is used to initiate the timing generator (5).

Multiplexer E7 in conjunction with comparator F7 (3) completes a hardware check on the desired sector after the proper track has been reached. When the correct sector has been selected, the sector compare signal "SC" from F7 is enabled. This is used to enable flip-flop G6 (6) to form CSC, which defines the period of data transfer whose format is shown in Figure 2-3.

Schematic 5 shows the origin of the timing for the Formatter operations. Counters D2, C1 and B1 form a chain which keeps track of the bits and words as they are transferred. Counter D2 counts the individual bits thus ensuring that its output at pin 15, BWTC, occurs at the end of each word. Various word lengths are accommodated by presetting D2 from the format decode logic (6).

Counters C1 and B1 count the words as they are transferred, finally activating signal SLC(N) when the last word has been transferred. This signal, in conjunction with either LSLCTC or SLC4, terminates BUSY (7) to end a block transfer. Figure 5-7 illustrates some of the key timing signals used in this section.

The preamble generator consists of multiplexers E2 and F2 to generate the signal PRE at F1 pin 11 (5). This section forms the preamble during a write sequence (Figure 2-4).

Schematics 6, 7 and 8 each show error detection logic. Schematic 6 detects Time Out Errors (TOE), Write Protect Errors (WPE), Preamble Compare Errors (PCE) and Format Errors (FE). Schematics 7 and 8 detect Rate Errors (RE) and Cylic Redundancy Code Errors (CRCE). Detailed operation of error detection logic can be found in Section 5-6.

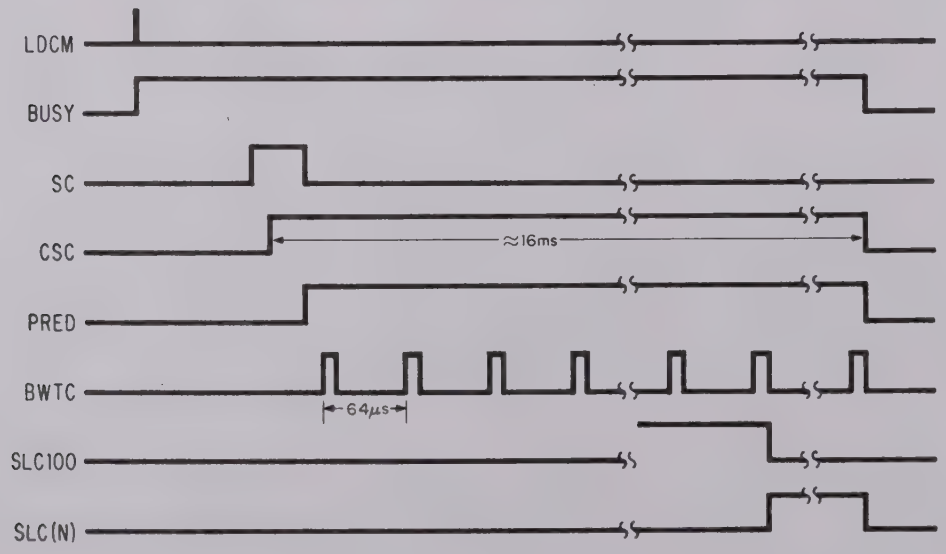


Figure 5-7. Typical Block Transfer Timing

5.4 DRIVE LOGIC

The Drive Logic (P/N 42555) block diagram is shown in Figure 5-8.

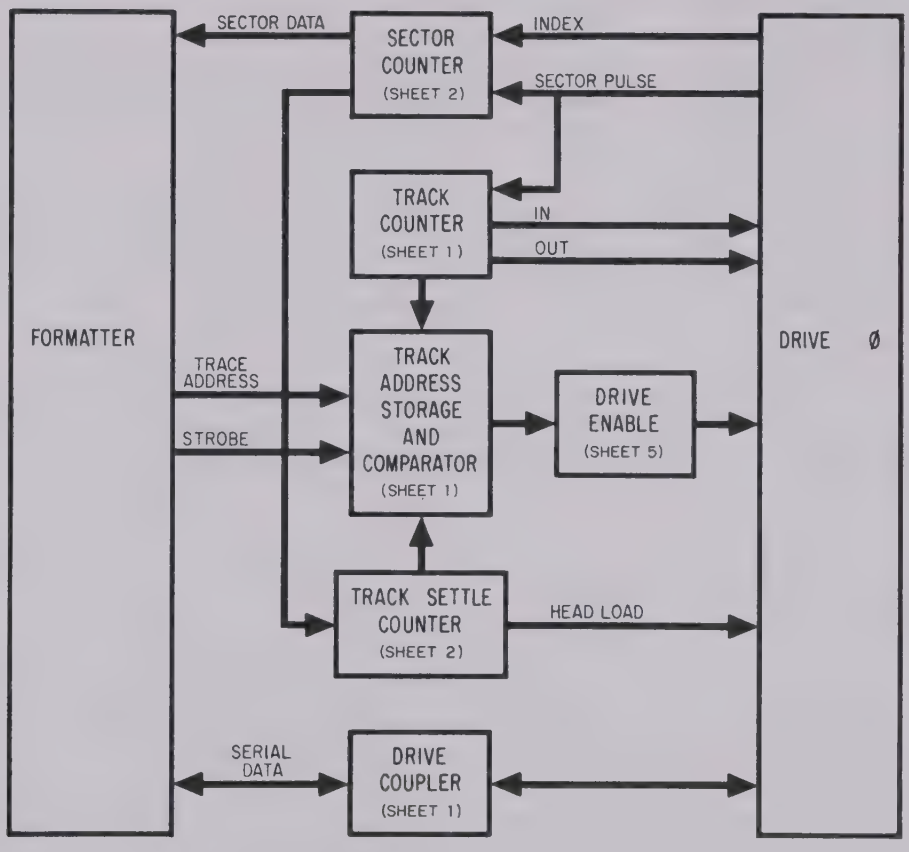


Figure 5-8. Drive Logic (Drive 0 Only)

The Drive Logic contains essentially two identical sections for drive 0 and 1. This discussion applies to the drive 0 section. Drive 0 and 1 signals from the Formatter are multiplexed over the same wires and directed to the proper section by logic on the board.

Counters D1 and D3 (1) monitor the track location of the head as it moves on the disk. Since the head drive motor is a stepper (with each step corresponding to a track), these counters simply count the number of in and out pulses sent to the drive.

Initialization is accomplished by a microswitch located at track zero called $\overline{\text{DTK00}}$. This switch sets flip-flop E2 (1) which was cleared by a restore command. When this flip-flop is set, counters D1 and D2 are held clear while comparator D2 forces the stepper motor to drive to track 0.

During a normal seek operation, latch C2 (1) stores the command track address. This address is then compared to the actual head location in comparators C1 and D2. D2 pin 7 or pin 5 will then be enabled depending upon whether the actual position is greater than or less than the desired position. Pulses will then be passed through gate E1 to drive the head to the correct location.

Counters H1 and H2 (2) provide a slight delay to ensure that the head has settled at the commanded position. These counters also enable shift register K2, which provides a head release signal after a 1.12 to 1.28 second delay.

Counters F1 and G1 monitor the sectors as the disk turns. The counters are initialized by the index pulse from the drive, called "D Index 0". The "Sector 0" signals are then counted to form the $\overline{SC0}$ through $\overline{SC4}$ timing signals, which are sector selected at the formatter.

IC G2 is a retriggerable one-shot which ensures the correct speed of the drive. Its period is just longer than the index 0 pulse rate of 160 milliseconds. IC G2 will never time out as long as correct drive speed is maintained.

5.5 DATA TRANSFER DESCRIPTION

The following narrative describes a typical data transfer (write) sequence. To identify the schematic location, the format (A/No) will be used in which A defines the assembly type (F=Formatter, C=Coupler, DL=Drive Logic) and No. the schematic number.

Assume the user desires to write a particular block of data in memory (say memory location (3000 3776) onto Drive #1 at track 25, sector 3. The following sequence of commands would be given:

```
LDMA-167202 = 3000
LDDA-167204 = 2253
LDCM-167200 = 1
```

The LDMA command loads the starting memory address of 3000 into memory address registers C6, B3, B4 and B5 on C/1 and C/2. The LDDA command will then generate an OSP command (C/6) which loads the DISK ADDRESS 2253 into track and sector latches F6, E3 and F4 on F/3. Finally, the LDCM command will initiate a write action by generating a COSP signal on F/7. COSP is a combination of OSP and REGSEL from C/6.

COSP generates a STRB to the Drive Logic, stores the Read/Write command in F3 (F/7) and sets the BUSY flip-flop consisting of gates L3 and G5 on F/7. The STRB signal loads the track address, stored in the

track and sector latches, into the track address latch C4 on DL/3. Note that the $\overline{STRB}$ is directed to C4 rather than to C2 (DL/1) by the unit select bit D1.

Comparators C5 and C6 on DL/3 will now force the head to drive to the correct track, which when found, will pass a $\overline{SEEKING}$ signal to the Formatter from B4 (DL/4). This enables the sector comparator F7 (F/3) in which the commanded Sector (3 in this case) will be compared to the sector timing signals from DL/4 via Selector E7 on F/3.

When the correct sector is found, SC will be enabled at F7-6. This will be synchronized in G6 (F/6) with the sector pulse $\overline{(SP)}$ to form CSC. In turn CSC develops a Write Enable (WE) to gates A1 (F/4) via gate N3 (F/8), initiating a field of 128 zeroes for bit synchronization as shown in Figure 2-3.

Just prior to CSC enable, counter C1 (F/5) is preset to a count of 8. Thus, the first LSLCTC pulse from C1 will occur after 8 words have been transmitted, which corresponds to the 128 zeroes. This first LSLCTC pulse will develop a GPRE signal in E1 (F/5). GPRE selects PRE in L4 (F/4) to provide the data to the Drive Logic board. PRE is the 10 word preamble shown in Figure 2-3 and developed in E2 and F2 (F/5).

NOTE: Figure 5-9 illustrates the timing relationships as described.

The first LSLCTC pulse also sets flip-flop H2 (F/5), which generates PRED. PRED in turn develops ENCCG on (F/8) which enables the CRC generator and selects the write data from K1 in selector L4 (F/4). A total of 256 data words will now be written.

Each of the 256 data words is passed from the Coupler to the Formatter each time a FLAG signal is developed by flip-flop K4 on (F/7). K4 is clocked high by BWTC from D2 on F/5. This occurs once each time a word is transferred. K4 is reset by OSP; the NPR timing signal from the Coupler.

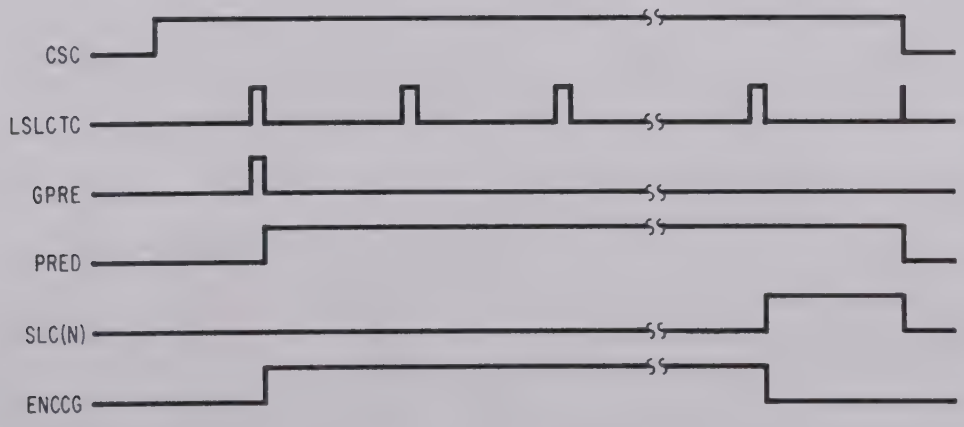


Figure 5-9. Typical Write Timing Relationships

OSP also loads each data word into latches C4, B7, E5 and D6 on F/1 and F/2, as they are received from the Coupler. BWTC then loads the latched data into shift registers D4, C7, E4, and E6 on F/1 and F/2 where it is shifted from E4 to K1 (F/4).

After the last data word is written, SLC(N) is enabled by the timing generator on (F/5). This terminates ENCCG on F/8, allowing the CRC code to be shifted from M4 (F/8) to L4 (F/4) and passed to DATA output to write the 16 bit CRC word on the disk.

The operation is completed when the BUSY flip-flop consisting of G5 and L3 on F/7 is reset. The first LSLCTC pulse after SLC(N) enabled causes the reset via L1 (F/7).

5.6 ERROR DETECTION LOGIC OPERATION

Bits locations are in RDST at address 167200.

Bit 1 CRCE CRC Error

The Cyclic Redundancy Check Error (CRCE) located on F/8 determines whether random errors have occurred during a Read/Write operation. This is accomplished by appending the data with a 16 bit word. This word represents the remainder of a division by a generator polynomial G(x). The G(x) used is a standard 16 bit Bi Sync protocol of the form $x^{16} + x^{15} + x^2 + 1$. When the block of data is read back, another remainder is generated from the recorded data. The check word initially written is then compared to the calculated remainder bit by bit. Any differences clear a flip-flop, generating a CRC error.

The divider, which generates the 16 bit check word, is a linear feedback shift register located on F/8 consisting of shift registers M1, M2, M3 and M4 and exclusive OR gates N1. Data to be divided enters N1 pin 1. After the data passes through the shift register the remainder is stored in M1 through M4. This data is then shifted out to form the CRC check character at the end of the data stream during a write operation. During a read operation, the recorded check character is compared to the calculated character at N1 pin 3. Any difference will clear flip-flop N4 which produces a CCE.

Bit 2 PCE Preamble Compare Error

The PCE is generated by flip-flop H2 on F/6 during a read cycle. During normal operation, a PC (Preamble Compare) signal is generated when the desired preamble matches that located on the sector being read. This action sets PRED high via flip-flop H2 on F/5. As long as PRED is high, flip-flop H2 on F/6 will not be cleared by SR15 and SR14 entering G5 to clock H2. However, if PC does not occur, PRED will remain low and flip-flop H2 will be cleared, generating a PCE.

Bit 3 RE Rate Error

An RE is generated when the computer fails to make a word transfer following a request to do so by floppy electronics. In normal operation K4-5 (F/7) generates a flag signal to the coupler card via B4 (F/7). The flag signal in turn generates an NPR request which must be answered before the next word is ready for transfer. When K4 is not cleared by a transfer action, K4-9 (F/7) will be clocked high by the next WORD time clock (BWTC) creating an RE. Figure 5-10 shows typical timing.

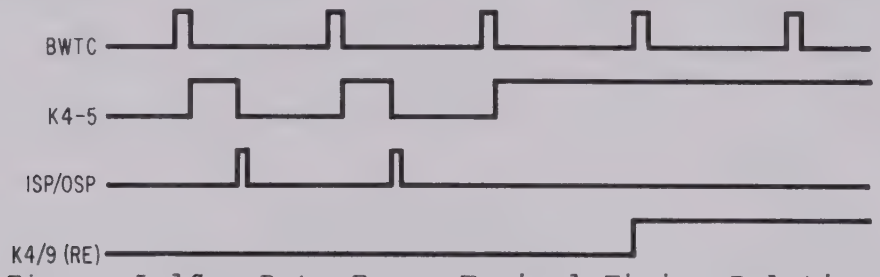


Figure 5-10. Rate Error Typical Timing Relationships

Bit 4 FE Format Error

An FE is generated by flip-flop G6 (F/6) when the CSC is not cleared before the arrival of the next sector pulse. In normal operation, SC at G6-2 (F/6) goes high indicating the desired track and sector have been found. CSC will then be generated at G6-5 by the next sector pulse. If CSC is not cleared before the next sector pulse arrives, G6-9 is clocked high forming the FE. This typically occurs when the preamble on the disk does not agree with the selected track and sector. Figure 5-11 illustrates typical timing.

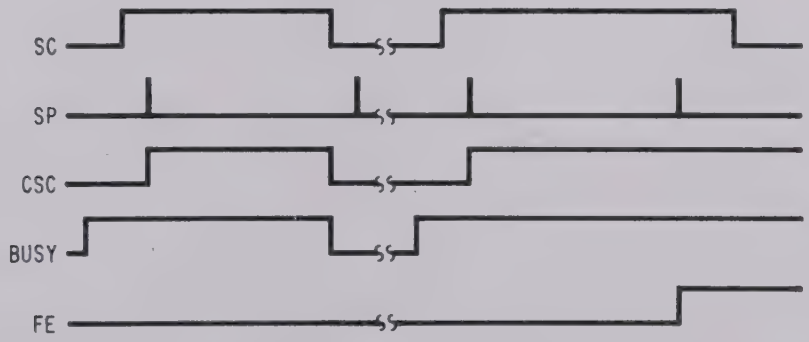


Figure 5-11. Format Error Typical Timing Relationships

Bit 5 WPE Write Protect Error

A WPE occurs in gate H3 (F/6) from a write protect signal ($\overline{WP}$) and a write command (C0). The $\overline{WP}$ signal originates in the disk drives and is derived by wire ORing the $\overline{WP0}$ and $\overline{WP1}$ signals on D/2 and D/4.

Bit 5 WPE Write Protect Error

A WPE occurs in gate H3 (F/6) from a write protect signal ($\overline{WP}$) and a write command (C0). The $\overline{WP}$ signal originates in the disk drives and is derived by wire ORing the $\overline{WP0}$ and $\overline{WP1}$ signals on D/2 and D/4.

Bit 6 TOE Timeout Error

A TOE is generated by counter K5 (F/6) when BUSY is not reset within 2.5 seconds after the start of an operation. In normal operation, BUSY is set high at the initiation of an operation such as read, write, etc. This allows K5 to begin counting $\overline{SC4}$, which is generated from count circuits on the Drive Logic board. If BUSY is not reset before 2.5 seconds, K5-15 goes high causing TOE.

Bit 13 BUS ERR Bus Error

Bus Errors originate on the coupler board in flip-flop F3 (C/5). This flip-flop is set as a result of the 5-microsecond one-shot E4 "timing out" before the PDP-11 responds to a MSYN during an NPR transfer. Normally the computer will acknowledge an MSYN with a SSYN which eventually creates a $\overline{CREQ}$ from one-shot E5 (C/5). SSYN takes state counters D3 and D2 (C/5) from state "11" to state "01". This drives the logic level at F3-2 (C/5) high via C8 so that when E4 times out, F3 will not change state.

SECTION 6
MAINTENANCE

WARNING

INFORMATION IN THIS SECTION IS FOR QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY FROM ELECTRIC SHOCK DO NOT REMOVE COVERS OR PERFORM ANY MAINTENANCE UNLESS YOU ARE QUALIFIED TO DO SO.

6.1 MAINTENANCE CONCEPT

ESI® has attempted to make maintenance and repair of the Model 1950 Flexible Disk Drive as easy as possible. Recommended maintenance for the ESI Model 1950 consists of periodic performance checks with the standard flexible disk diagnostic program. To verify the unit's performance, the diagnostic should be run following installation, and periodically thereafter.

Similarly, if a malfunction is suspected, use the diagnostic program as a guide to isolating the malfunction to one particular section of the hardware. Section 4 describes the diagnostic program and procedures. Once an error message is printed out for any given test, that information can be analyzed with the information in the diagnostic description, in order to isolate the malfunction to one of five probable areas:

1. Disk drive assembly (two per chassis unit)
2. Power supply (one per chassis unit)
3. Drive logic card assembly (one per chassis unit)
4. Formatter card assembly (one per system in the main recorder chassis unit)
5. Interface card assembly (one per system; located in the PDP-11 Computer)

If a malfunction is isolated to one of these subassemblies, remove it from the system, and replace it with a spare subassembly that is operating properly. Return the malfunctioning subassembly to the factory for repair. The disassembly procedures are included in this section of the manual; follow the procedures for removing any of the subassemblies.

Section 6.2, Flexible Disk Drive Alignment, contains information on preventive and corrective maintenance for the 195Ø drive. Head Cleaning, section 6.2.3.2, is recommended every six months or more often if the operating environment is especially dirty. In general, when the 195Ø encounters problems in either reading or writing to a disk, first perform the head cleaning procedure; then, if the problem persists, do the appropriate disk drive alignment procedures.

6.2 FLEXIBLE DISK DRIVE ALIGNMENT

6.2.1 Description

The Flexible Disk Drive alignment program FDTST.SAV is an ESI Pascal program which provides procedures for the maintenance and alignment of the ESI Model 195Ø Dual Flexible Disk Drive.

The program can be loaded into the computer's main memory through either one of the drives or some other storage device. Each procedure contains detailed instructions and will prompt the user for information needed for execution and will therefore not be repeated here.

In the case that the system must be booted on the 1950 but FDØ is inoperative, do the following:

STEP 1. Read sections 6.3 and 6.3.1 for disk drive disassembly instructions.

STEP 2. Interchange disk drive assembly Ø with disk drive assembly 1.

STEP 3. Restore AC power. Attempt to boot the system.

STEP 4. If the problem persists (drive Ø was not at fault), the alignment program can be run using the procedures in section 6.2.2.2, Head Positioning.

FDTST procedures can be accessed through a command dispatch (FD>) by typing a procedure identifier. See the block diagram below.

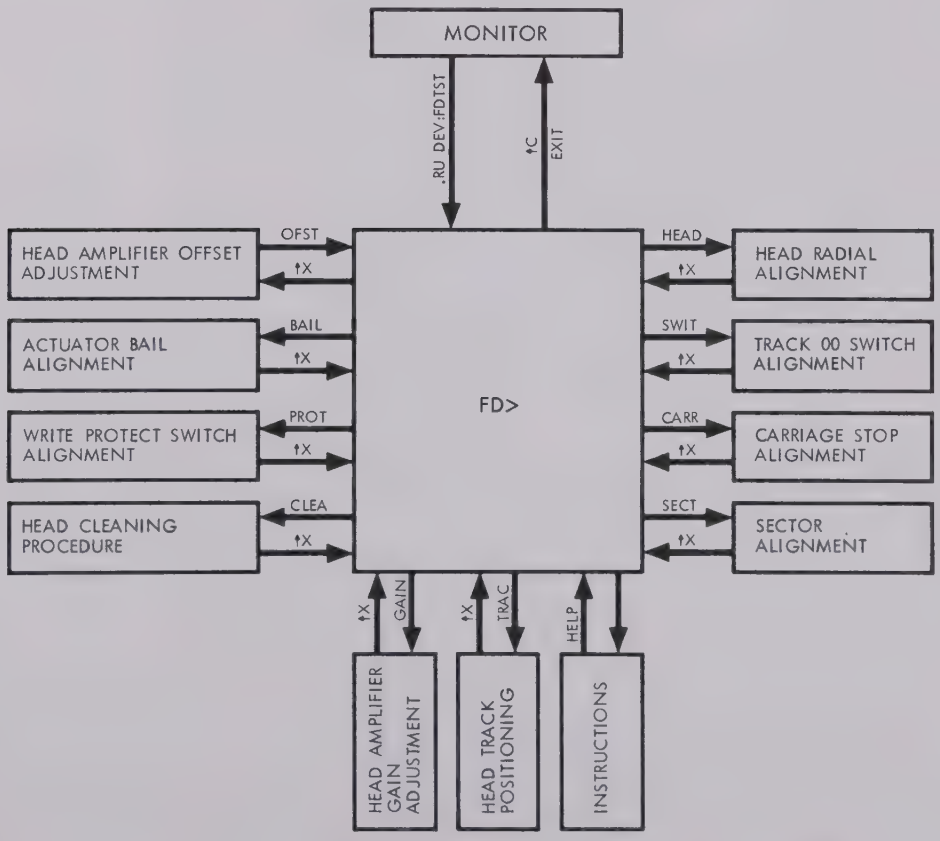


Figure 6-1. FDTST Command Block Diagram

6.2.2 FDTST Program Operation

6.2.2.1 Program Description

To run the program, type:

.R FDTST↵ OR .RU DEV:FDTST↵

NOTE: ↵ means carriage return.

The system will respond with a heading and the prompt FD>, which is the command dispatch mode. The four-letter procedure identifier for the desired procedure may now be entered. The procedure identifiers are:

BAIL - Actuator bail alignment
PROT - Write protect switch alignment
CLEA - Head cleaning procedure
HEAD - Head radial alignment
SWIT - Track ØØ switch alignment
CARR - Carriage stop alignment
SECT - Sector alignment
GAIN - Head amplifier gain adjustment
TRAC - Track selection
HELP - Instructions

HEAD is a prerequisite for SWIT, CARR, SECT.

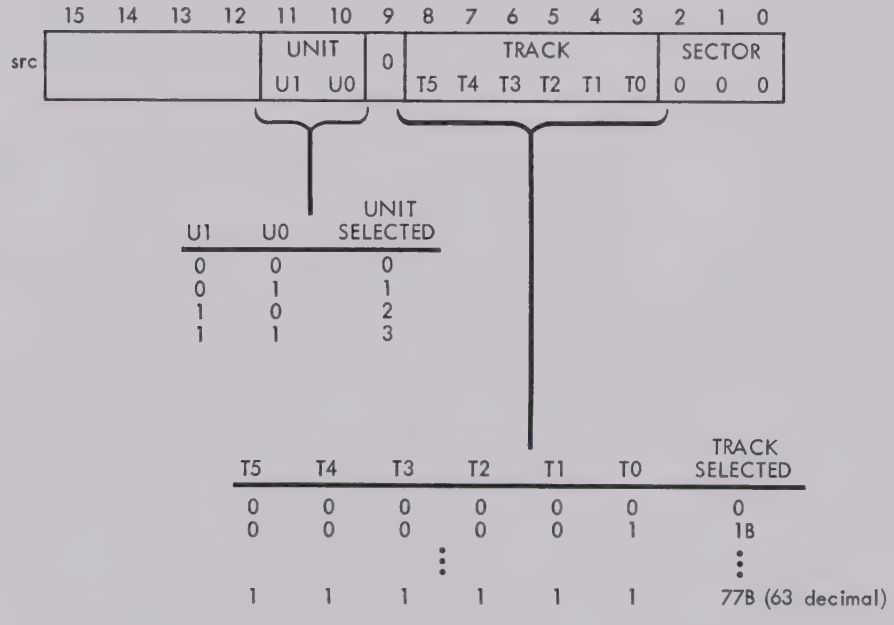
6.2.2.2 Head Positioning

The head can be positioned at any track by using the emulator. Refer to the User's Guide for your computer for information about the emulator. The sequence of operation is:

NOTE: In Pascal programming, octal numbers are written with a "B" as the last character. Example 14B (octal) = 12 (decimal).

STEP 1. Deposit drive and track information (octal integers) into disk address 167204.

STEP 2. Deposit 103 into command address 167200.



As an example, the following operation will position the head on track 37B of unit 1.

```
L    167204
D    2370          (Track 37B of unit 1 selected)
L    167200
D    103           (Seek to track and unit specified)
```

6.2.3 Hardware Descriptions and Alignment Procedures

NOTE: Only qualified personnel should attempt the following alignment procedures. The alignment information described below is for the emulator mode of operation only. For program operation, refer to instructions contained in the program.

6.2.3.1 Equipment Required

	ESI Part Number
Flexible Disk Drive Alignment Package:	47089
- Field Service Alignment Package	47091
- Cleaning Kit	46666

Oscilloscope with differential inputs and external sync

Digital voltmeter

6.2.3.2 Head Cleaning

Sometimes a malfunction may be due to a dirty head. Clean the head as often as necessary and before attempting the alignment procedures with isopropyl alcohol and wipe dry with a lint free cloth. The following applies:

STEP 1. Check the head load pad for wear and proper position. It is important that the pad is positioned centrally over the head contact area.

STEP 2. To replace the pad, carefully remove the backing and place the pad felt-side down and center it on the head. Lower the load arm gently onto the pad and apply enough pressure to pick up the pad. Ensure that the pad is firmly attached by applying pressure on the pad with a piece of clean material.

STEP 3. For initial cleaning or removal of light build-up, brush in the direction of the head slots with a lint-free applicator wetted with isopropyl alcohol. Wipe dry with cleaning cloth (supplied with cleaning kit) in the direction of the head slots. Inspect head surface. A light, discolored burnished area, around the center of the head is normal. Repeat the process as often as necessary.

FOR EXTREME BUILD-UP*

STEP 4. Insert cleaning disk into drive.

STEP 5. Step the head back and forth across the surface of the cleaning disk by repeatly and alternately grounding TP26 (in) and TP27 (out). Continue this operation for 30 minutes.

*Not recommended for normal cleanings

6.2.3.3 Head Load Actuator Assembly

Description

The Head Load Actuator Assembly consists of a solenoid assembly with an armature extension that operates a bail and wiper pad. The purpose of the assembly is to control the action of the load arm, which is spring-loaded to press the disk in the cartridge guide against the head mounted on the carriage assembly. When the solenoid is de-actuated, armature spring action moves the bail away from the disk. The bail contacts the load arm tab, and the bail travel moves the load arm pressure pad out of contact with the disk. The solenoid is energized by the -LOAD HEAD signal. When the solenoid is actuated, the armature moves the bail toward the disk, which places the wiper pad lightly in contact with the cartridge, and disengages the bail from the load arm tab. The load arm spring moves the released load arm toward the disk, and the load arm pressure pad presses the disk against the head. The position of the bail on the armature extension is adjustable and must be adjusted so that the bail is out of contact with the load arm tab when the solenoid is actuated but accomplishes the required amount of load arm travel when the solenoid is deactuated. The load arm spring must be capable of supplying a pressure of 10 to 18 grams between the load arm pressure pad and the head.

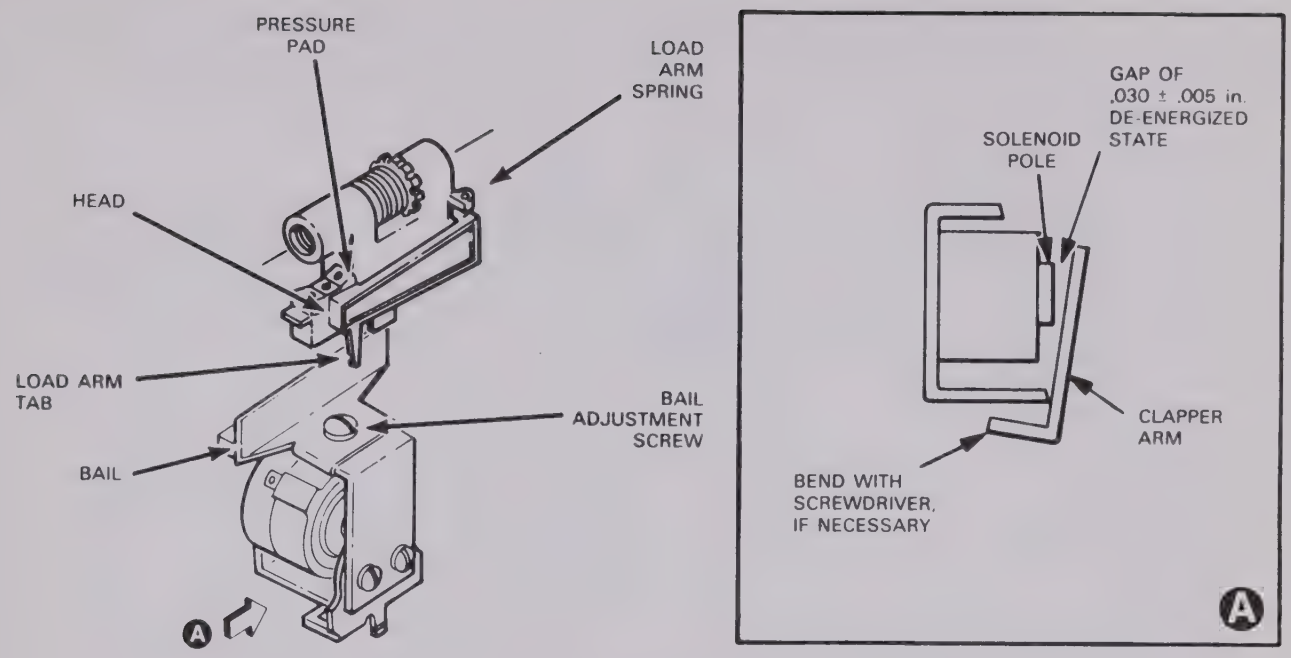


Figure 6-2. Head Load Actuator Components

Actuator Bail Alignment

STEP 1. With the head unloaded (door opened), verify that the bail moves the load arm so that the pressure pad will not contact the disk during disk interchange.

STEP 2. With the head loaded (door closed), verify that the bail stays clear of the load arm tab.

STEP 3. Verify that conditions described in steps 1 and 2 are true at tracks Ø, 31, and 63. (See head positioning instructions.)

STEP 4. If requirements of steps 1 and 2 are not met, adjustments could be made by bending the bottom of the clapper arm with the head loaded for a gap of Ø.Ø3Ø (±Ø.ØØ5) inch between the solenoid pole and the clapper arm and/or by loosening the actuator bail adjustment screws with the head loaded for clearance of Ø.Ø15 (±Ø.ØØ5) inch at both ends of the bail.

Type the following, while the computer is in the emulator mode, to position the head on the desired track:

```
Drive Ø:  L  167204
          D  Ø        (for Drive Ø, Track Ø; or 2ØØØ for Drive 1,
                       Track Ø; or 37Ø for Drive Ø, Track 31; or 237Ø
                       for Drive 1, Track 31; or 77Ø for Drive Ø, Track
                       63; or 277Ø for Drive 1, Track 63)
          L  167200
          D  1Ø3
```

6.2.3.4 Write Protect Switch

Description

The Write Protect Switch is a spring-loaded, level-actuated switch with contacts normally open (no write-protected disk installed in drive). With a write-protected disk installed, the switch is activated to its closed position. This prevents WRITE ENABLE from being initiated and provides a write-protect status to the using system.

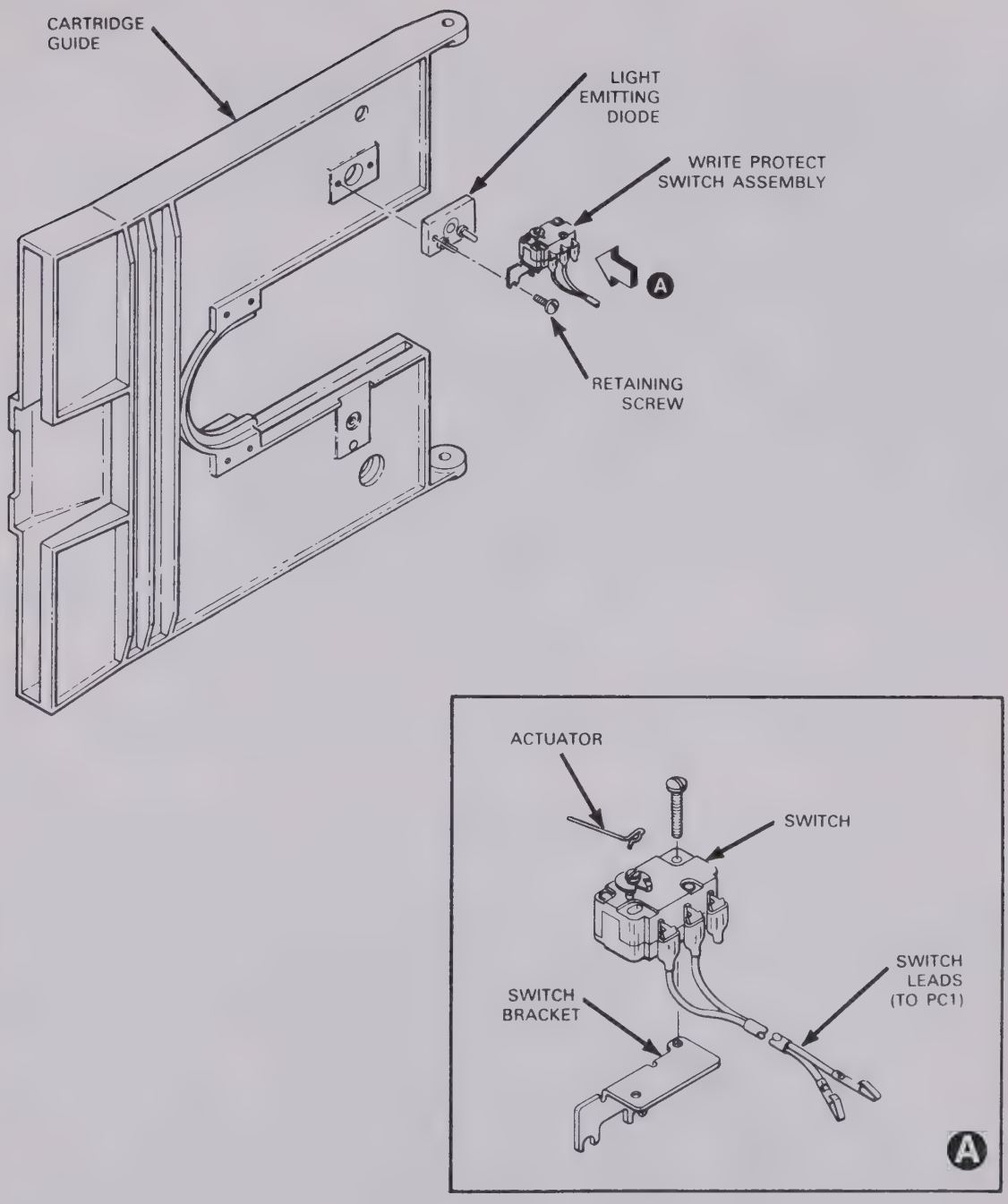
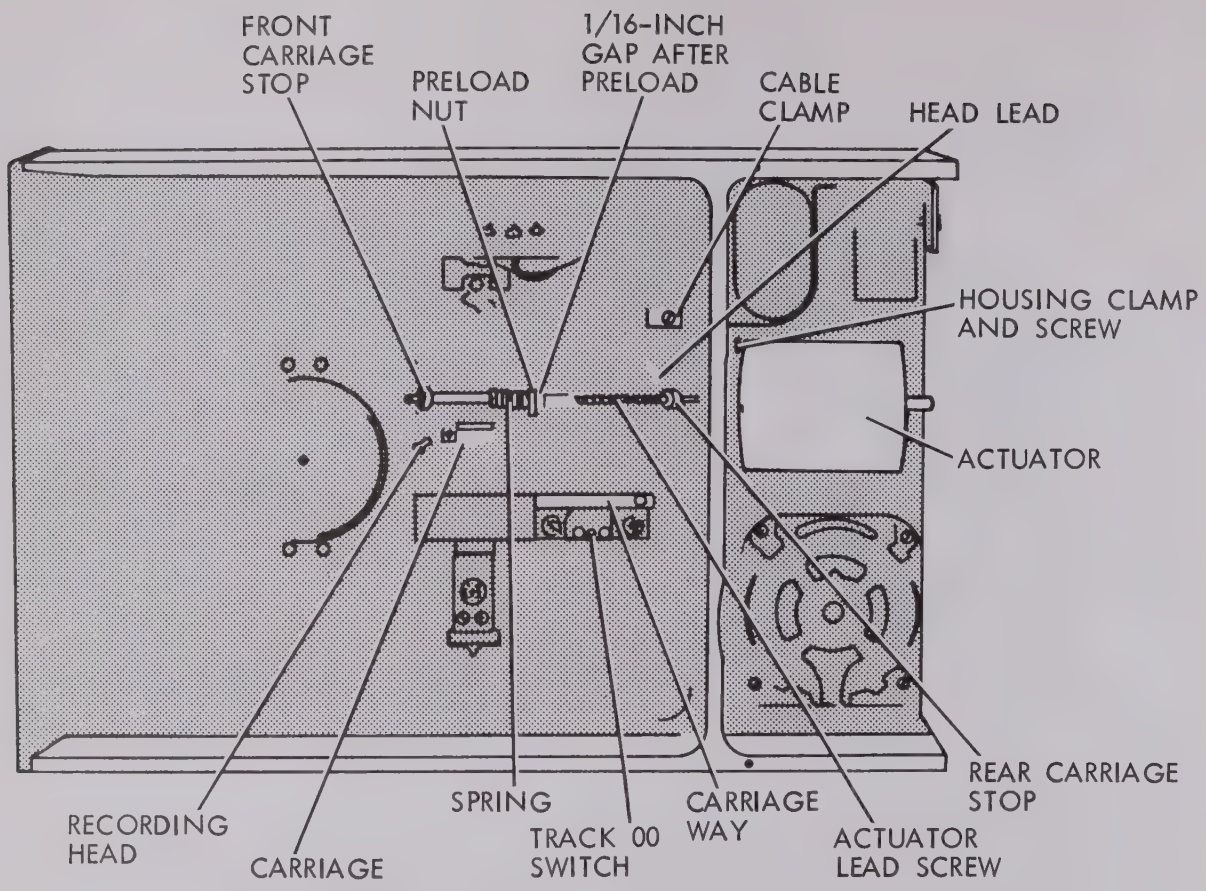


Figure 6-3. Write Protect Switch



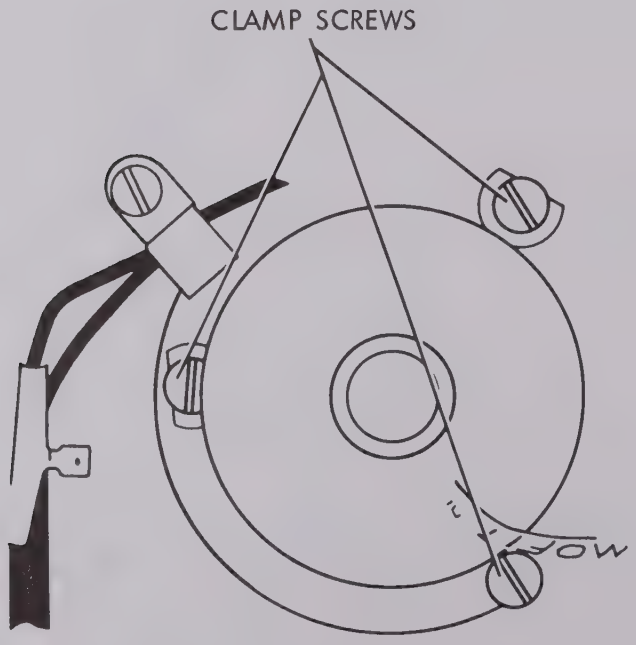


Figure 6-4. Head Position Actuator Clamp Screws

Alignment

STEP 1. Adjust the switch so the actuator just touches the left side of the cartridge guide hole (Figure 6-3). This may be accomplished by loosening the switch-bracket-to-cartridge-guide retaining screws and moving the switch. If this movement does not provide sufficient adjustment latitude, bend the wire switch actuator to provide for proper adjustment.

STEP 2. Check that the switch is in the open condition without a disk cartridge installed in the drive, and that the switch actuates to the closed condition when a write-protected disk is installed. The switch should actuate 1/32 inch (minimum) before the cartridge is fully inserted into the cartridge guide, and deactuate at or before the cartridge is extracted 1/8 inch.

6.2.3.5 Head Carriage and Head Position Actuator Assemblies

Description

The Head Carriage assembly, along with the Track Position Actuator, and Track ØØ Switch assemblies make up the track accessing subassembly of the drive. The purpose of this assembly group is to provide file access by track address.

The recording head is mounted on a carriage that travels parallel to a horizontal radius of the vertically mounted disk. The carriage is driven toward or away from the disk center by a rotating screw on which the carriage is mounted. The screw is rotated in either direction by the head position actuator. This actuator is a stepping motor that rotates the screw in 15 degree increments. The linear head travel resulting from one rotation increment is equal to the center-to-center distance between two adjacent tracks on the disk (approximately Ø.Ø2Ø inch). Track accessing depends upon the initial alignment of the carriage on the screw so that head is radially positioned over a track centerline. Carriage stops are mounted on either end of the screw to prevent inadvertent carriage overtravel. The stops must be correctly positioned after the head radial alignment is complete.

Head Radial Alignment

The following steps should be followed for this alignment.

STEP 1. Place the alignment disk (Memorex Part No. 3Ø7ØØ7) into the drive assembly to be aligned. Allow five minutes to stabilize temperature.

STEP 2. Type the following information for the drive assembly being aligned:

DRIVE Ø		DRIVE 1
L 167204		L 167204
D 370	OR	D 2370
L 167200		L 167200
D 103		D 103

STEP 3. Assure phase Ø2 of the stepping motor is energized. (TP17 is <+Ø.3VDC.)

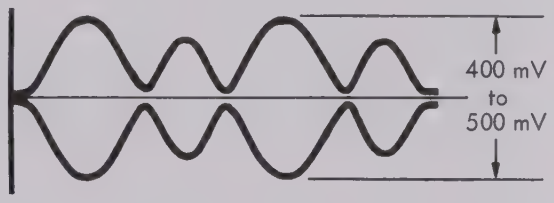
STEP 4. Adjust the oscilloscope to:

a. Ø.2 volts per division
b. Sweep rate 2Ø milliseconds per centimeter
c. External trigger - triggered sweep
d. Sweep control to ADD

STEP 5. Connect the oscilloscope to the following test points:

a. CHAN 1 to TP1
b. CHAN 2 to TP2
c. External Trigger to TP1Ø

STEP 6. You should see several lobes on the oscilloscope.



STEP 7. The lobes should be approximately equal (±25%) in amplitude.

STEP 8. The alignment is made by loosening the stepper motor mounting screws. Rotate the motor until the lobes are equal in amplitude.

STEP 9. Tighten the screws and check to see that the alignment is still good, as the motor may move when the screws are tightened.

Carriage Stop Alignment

STEP 1. Type the following information for the assembly being aligned.

DRIVE Ø		DRIVE 1
L 167204		L 167204
D Ø	OR	D 2ØØØ
L 167200		L 167200
D 1Ø3		D 1Ø3

STEP 2. Adjust the rear carriage stop until there is Ø.ØØ7 inches between the carriage stop and the carriage.

STEP 3. Type:

DRIVE Ø		DRIVE 1
L 167204		L 167204
D 77Ø	OR	D 277Ø
L 167200		L 167200
D 1Ø3		D 1Ø3

STEP 4. Adjust the front carriage stop until there is Ø.ØØ7 inches between the carriage stop and the carriage.

NOTE: In the preceding emulator programs, 167204 refers to the Disk Address and 167200 refers to the Command Word.

Track ØØ Switch Alignment

NOTE: Radial head must be in alignment for the following to be valid.

To verify switch operation make measurements at pin 11 of 5D (74Ø3). At Tracks ØØ and Ø1, pin 11 should be at high logic level. At all other tracks it should be at low logic level.

STEP 1. Position the head at Track Ø1 (see Section 6.2.2.2 or instructions below for head positioning) [TP17 (Ø.3 volt)]; loosen the two bracket screws and slide the bracket to the right so that the switch is deactuated.

STEP 2. Slowly slide the bracket to the left just enough to actuate the switch. Verify that the switch is actuated.

STEP 3. Tighten the bracket screws while holding the switch in position.

STEP 4. Position the head at Track Ø2 and verify that TP15 is less than Ø.3 volt.

STEP 5. Verify that the switch is deactivated; if not, slightly loosen the left-hand bracket screw and gently nudge the bracket downward until the switch is deactivated. (Switch is usually deactivated if steps 4 and 5 were performed satisfactorily.)

STEP 6. Alternately position the head on tracks Ø1 and Ø2 to verify switch operation.

Type in the following to position the head at Track Ø1:

```
L 167204
D 1Ø (or 2Ø1Ø for Drive 1)
L 167200
D 1Ø3
```

To position the head at Track Ø2, type:

```
L 167204
D 2Ø (or 2Ø2Ø for Drive 1)
L 167200
D 1Ø3
```

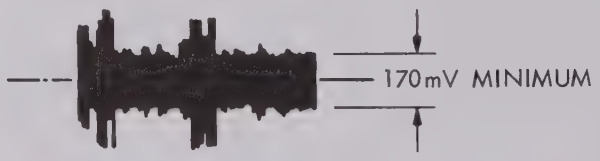
Head Amplifier Gain Adjustment

STEP 1. Set up oscilloscope as follows:

a. Channel 1 to TP1, 200mV/div
b. Channel 2 inverted to TP2, 200mV/div
c. External trigger to TP9
d. Sweep control to ADD
e. Sweep rate to 5ms/div

STEP 2. Run "GAIN" of FDTST.SAV.

STEP 3. Adjust R5 (see Figure 6-5) to obtain 170mV minimum at track 63 and 1.6V maximum at track 0. See diagram below.

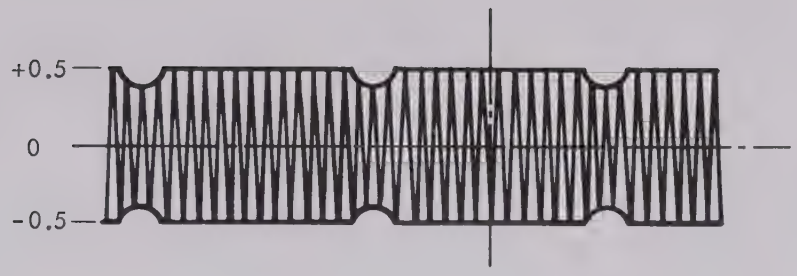


An alternate method is to adjust R5 for 200mV at track 63 and not check track 0.

Head Amplifier Offset Adjustment

STEP 1. Set up oscilloscope as follows:

a. Channel 1 to TP19, .5V/div
b. Channel 2 to TP20, .5V/div
c. External trigger to TP9
d. Sweep control to ADD
e. Sweep rate to 5ms/div
f. Center sweep on zero reference line



STEP 2. Adjust R1Ø4 (see Figure 6-5) to center the signal envelope around the zero reference line.

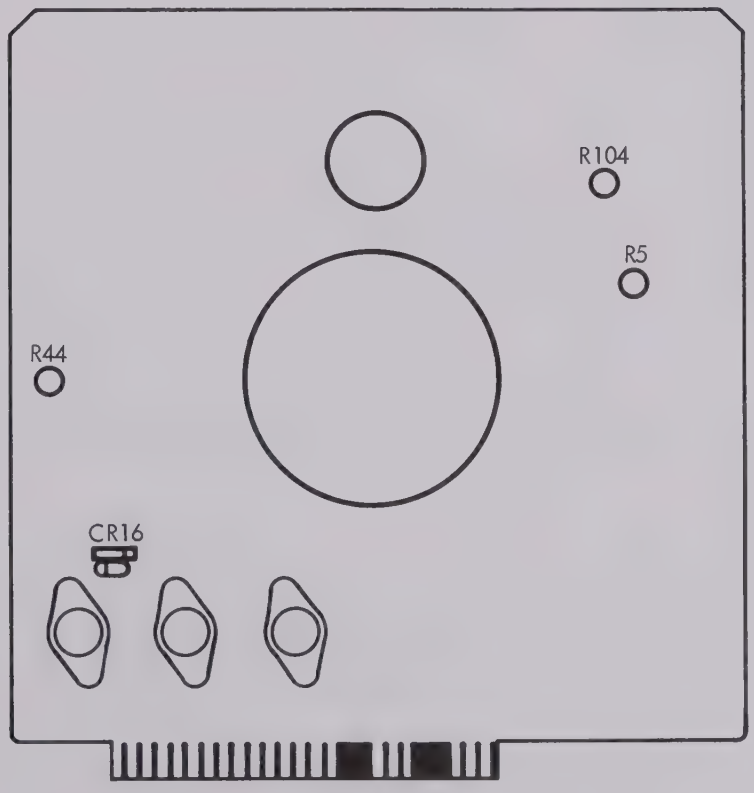


Figure 6-5. Read/Write/Access Circuit Card

6.2.3.6 Index and Sector Sensing Components

Description

These components consist of the Light Emitting Diode assembly, mounted on the front of the cartridge guide, and the Photo Transistor assembly, mounted behind the cartridge guide. The line of sight connecting these two components is perpendicular to the plane of the disk and intersects the disk at the circle formed by the 32 sector holes and the index hole. When the disk is rotating, invisible infrared light emission from the light emitting diode actuates the photo transistor, which generates a 5-volt pulse, each time one of the Ø.1Ø inch diameter holes in the disk exposes the photo transistor to the light emitting diode. An adjusting screw on the Photo Transistor assembly permits positioning of the photo transistor along the arc of the disk holes so that the leading edge of the index/sector pulse occurs simultaneously with coincidence of the recording head and the geometric index or sector radius on the disk. This will assure that the leading edge of the sector pulse will occur simultaneously with the beginning of the physical sector. This alignment is accomplished with the aid of the alignment disk. The initial transistion peak of the burst occurs 1ØØµs after the leading edge of the SECTOR pulse.

Sector Alignment

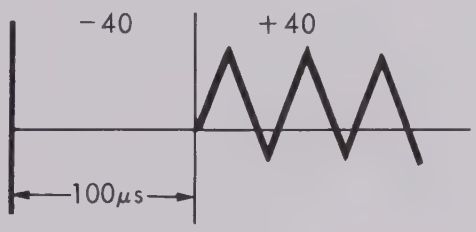
STEP 1. Install jumper (Memorex Part No. 2Ø4296) between READ/WRITE and connector pins on the drive circuit card.

STEP 2. While the computer is in the EMULATOR mode, type the following information for the drive assembly being aligned:

DRIVE Ø		DRIVE 1
L 167204		L 167204
D 70	OR	D 2070
L 167200		L 167200
D 103		D 103

STEP 3. Set the oscilloscope sweep rate to 20µs per centimeter.

STEP 4. You should see a burst approximately 100µs ±40µs after the start of the sweep.



STEP 5. Make note of the time at which the burst begins.

STEP 6. Type the following:

DRIVE Ø		DRIVE 1
L 167204		L 167204
D 70	OR	D 2070
L 167200		L 167200
D 103		D 103

STEP 7. Again, the sector burst should be 100µs ±40µs. Note the time at which the burst begins.

STEP 8. Each burst should begin symmetrically about the 100µs mark.

Example: If the burst from track 7 starts at 90µs then the burst from track 70 should start at 110µs.

STEP 9. To adjust the sector burst, turn the screw located behind the access hole in the top of the drive assembly.

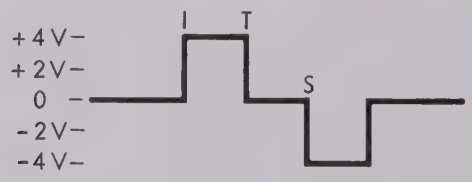
STEP 10. Repeat as necessary to attain symmetry.

Index Timer Adjustment

STEP 1. Set up oscilloscope as follows:

a. Channel 1 to TP7, 2V/div
b. Channel 2 to TP8, 2V/div
c. External trigger to TP9
d. Sweep control to ADD
e. Sweep rate to 0.5ms/div

STEP 2. Adjust R44 (see Figure 6-5) to locate T midway between I and S as shown below.



6.3 RECORDER CHASSIS UNIT DISASSEMBLY

WARNING

DISCONNECT AC POWER TO THE DISK DRIVE TO AVOID PERSONAL INJURY AND/OR DAMAGE TO THE EQUIPMENT.

The drive logic card, the formatter card, the power supply and the disk drive assemblies are located in the chassis unit; for access, use the following procedure:

STEP 1. Remove the screws on the front panel of the 1950 disk drive assembly, and slide the chassis unit out from the rack.

STEP 2. Remove the top cover of the chassis. Remove the Phillips-head cover retainer screws at the side and top of the chassis. After removing the screws, lift the cover off the chassis.

6.3.1 Disk Drive Assembly Removal

WARNING

DISCONNECT AC POWER TO THE DISK DRIVE TO AVOID PERSONAL INJURY AND/OR DAMAGE TO THE EQUIPMENT.

STEP 1. Disconnect the two cable connectors at the rear of each drive assembly. One of the connectors has thumb screws that secure it to the drive assembly; loosen the thumb screws and slide the connector off. The other connector is not secured, and slides off.

STEP 2. Slide drive assembly out from the front of the disk recorder chassis assembly.

6.3.2 Drive Logic and Formatter Cards Removal

STEP 1. Disconnect cables connected to J1, J2, J3 and J4 on the rear panel of the chassis. Remove the line cord that connects AC power to the chassis.

BEFORE ATTEMPTING TO REMOVE THE FORMATTER OR DRIVE LOGIC CIRCUIT CARDS, BE SURE TO DISCONNECT ALL 115VAC LINE POWER FROM THE DISK RECORDER CHASSIS UNIT.

STEP 2. To remove the formatter card, pull straight up. The formatter card should come loose.

STEP 3. Remove the four nylatches that secure the drive logic circuit card, and lift it from the recorder chassis assembly.

6.3.3 Interface Card Removal

If trouble is isolated to the interface card, remove it from the PDP-11 computer. Remove the covers of the computer and locate the ESI I/O interface card assembly. When replacing the interface card, make sure that it is positioned correctly in the guidance slots, and that the connectors are aligned properly.

6.4 FACTORY REPAIR

After a subassembly has been removed, ship to:

Electro Scientific Industries, Inc.
13900 N. W. Science Park Drive
Portland, Oregon 97229
Attention: Service Department

For additional information, write, call or telex ESI at the following numbers:

Telephone: ESI - (503) 641-4141
ESI Field Service - (503) O-HELP-ME
Telex: 15-1246

When shipping any unit or component, send the following information:

1. Name and address of owner.

2. Brief discussion of symptoms or trouble.

3. If possible, send the name and telephone number of someone familiar with the problem, and who may be contacted if more information is needed.

4. Special shipping instructions, if any. Include your return shipping address and department mail address, if necessary.

6.5 PACKING/SHIPPING INSTRUCTIONS

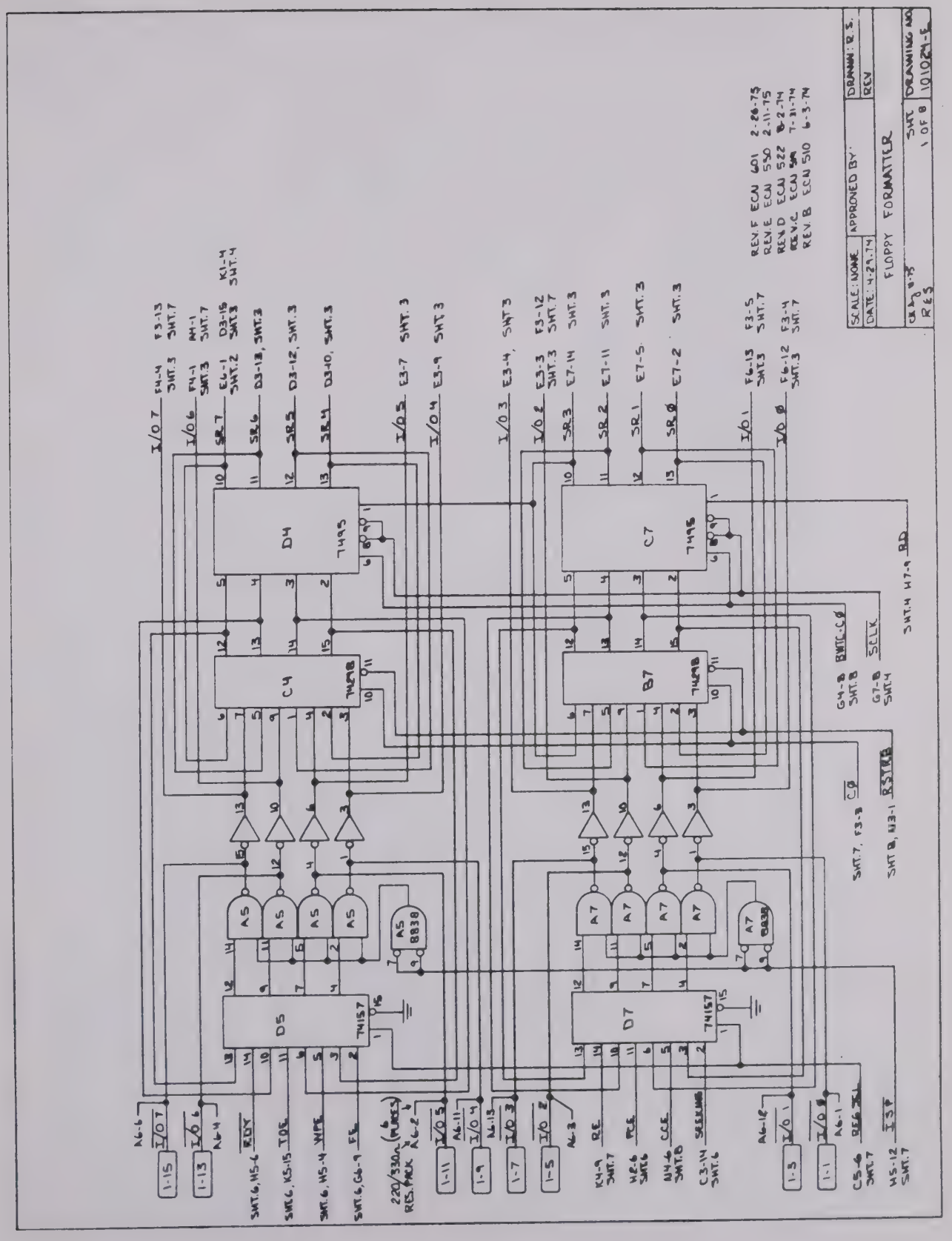
If the entire system is to be shipped, pack it according to the instructions in Section 3.3. If a subassembly is being shipped, use the following packing procedure:

STEP 1. Wrap the subassembly in plastic.

STEP 2. Place the subassembly in a sturdy container; add packing material around all sides of the subassembly.

STEP 3. Seal the shipping container with reinforced tape.

STEP 4. Mark the shipping container to indicate that it contains fragile electronic equipment.


FLOPPY FORMATTER
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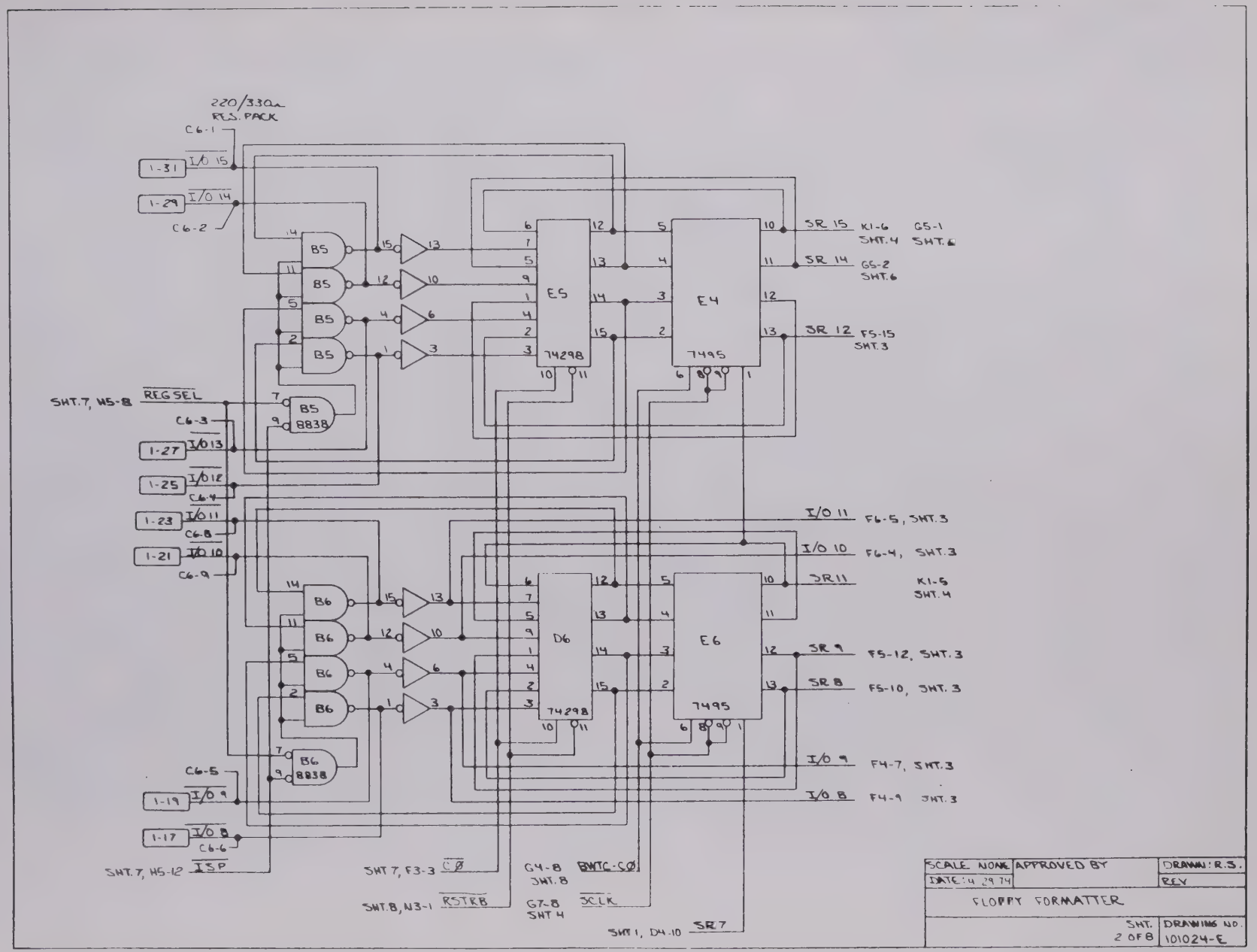
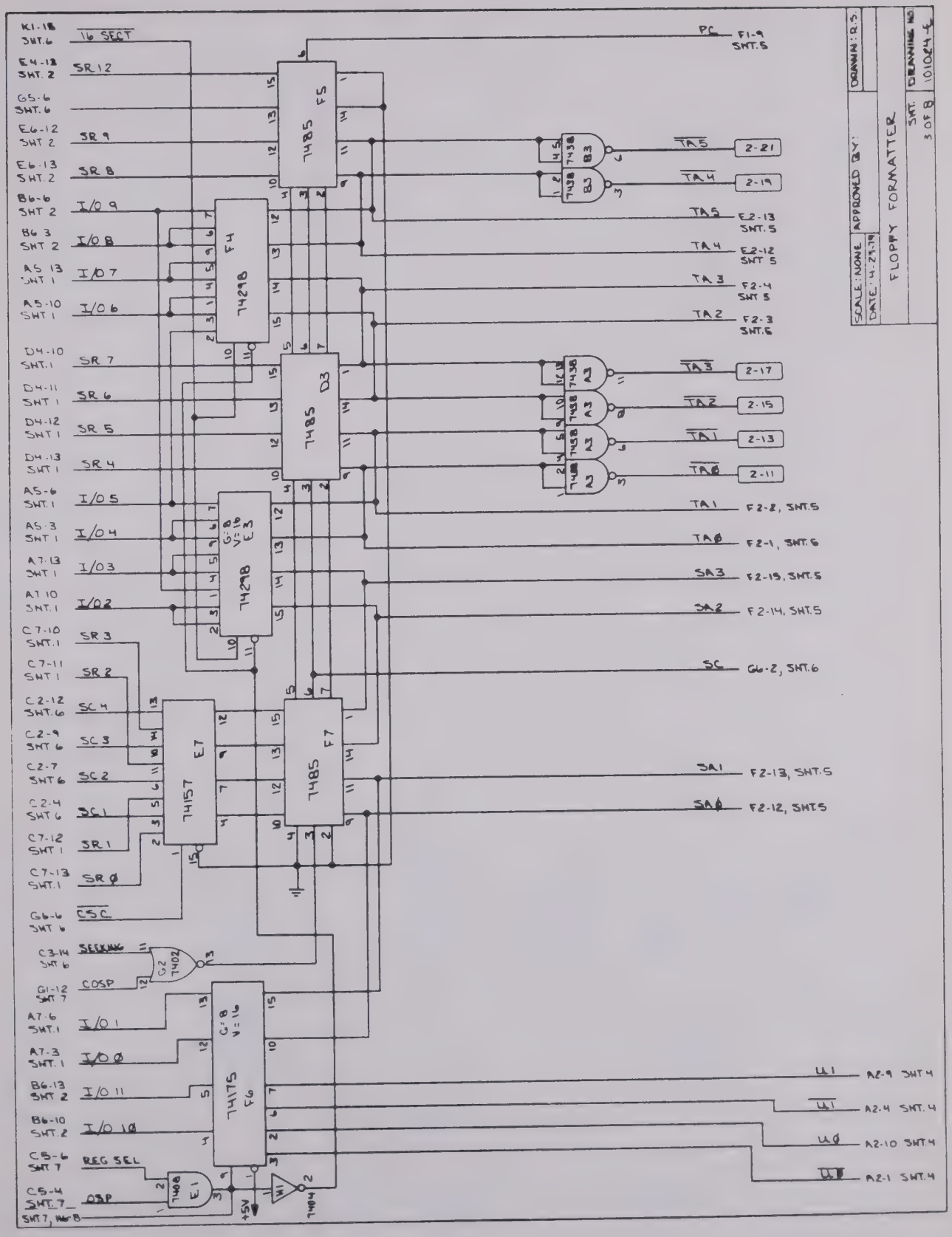
APPROVED BY:
DRAWN: R.S.
REV
SHT.
1 OF 8
DRAWING NO.
101021-F
REV. F ECN 601 2-26-75
REV. E ECN 530 2-11-75
REV. D ECN 522 12-2-74
REV. C ECN 514 7-31-74
REV. B ECN 510 6-3-74
D4
7495
C4
74298
D5
74157
C7
7495
B7
74298
D7
74157
A5
A7
8838
9838
I/O 7
I/O 6
I/O 5
I/O 4
I/O 3
I/O 2
I/O 1
I/O 0
SR.7
SR.6
SR.5
SR.4
SR.3
SR.2
SR.1
SR.0
220/330Ω (6 RES. PACK)
SHT.4 H7-9 BD
SHT.7, F3-9 C0
SHT.8, H3-1 RESET
G4-8 BWTC-C0
G7-8 SELK


220/330Ω RES. PACK
C6-1
1-31 I/O 15
1-29 I/O 14
C6-2
B5
B5
B5
B5
B5 8838
E5
74298
E4
7495
SR 15 K1-6 SHT.4 G5-1 SHT.6
SR 14 G5-2 SHT.6
SR 12 F5-15 SHT.3
SHT.7, H5-8 REG SEL
C6-3
1-27 I/O 13
1-25 I/O 12
C6-4
1-23 I/O 11
C6-8
1-21 I/O 10
C6-9
I/O 11 F6-5, SHT.3
I/O 10 F6-4, SHT.3
SR 11 K1-6 SHT.4
B6
B6
B6
B6
B6 8838
D6
74298
E6
7495
SR 9 F5-12, SHT.3
SR 8 F5-10, SHT.3
C6-5
1-19 I/O 9
1-17 I/O 8
C6-6
I/O 9 F4-7, SHT.3
I/O 8 F4-9 SHT.3
SHT.7, H5-12 ISP
SHT.7, F3-3 CØ
G4-8 SHT.8 SWTC-CØ
SHT.8, N3-1 RSTRB
G7-8 SHT.4 SCLK
SHT.1, D4-10 SR7
SCALE NONE
APPROVED BY
DRAWN: R.S.
DATE: 4 29 74
REV
FLOPPY FORMATTER
SHT. 2 OF 8
DRAWING NO. 101024-E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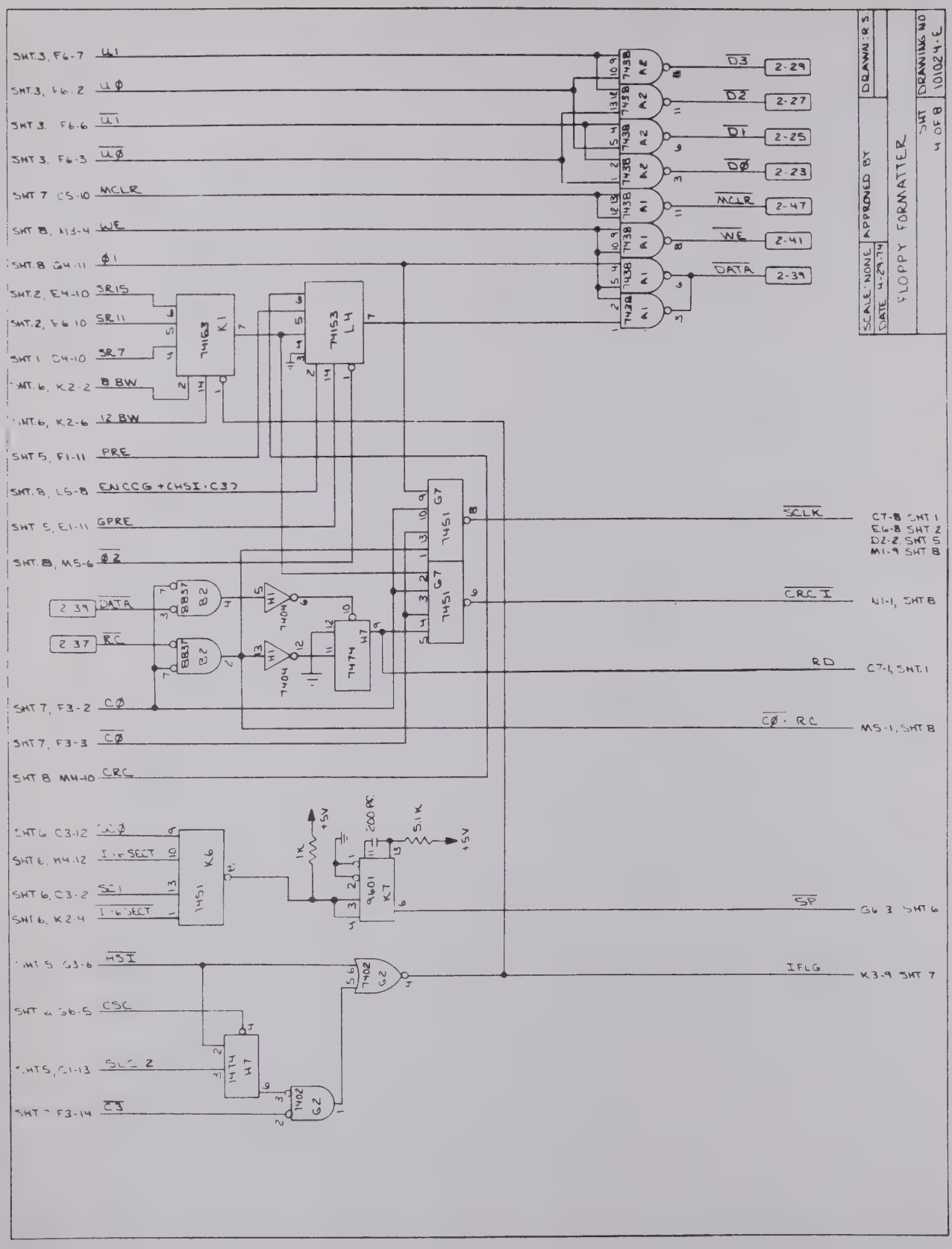
1010629-6
SHT. 3 OF 8
16 SECT
SR12
SR9
SR8
I/O 9
I/O 8
I/O 7
I/O 6
SR 7
SR 6
SR 5
SR 4
I/O 5
I/O 4
I/O 3
I/O 2
SR 3
SR 2
SC 4
SC 3
SC 2
SC 1
SR 1
SR Ø
CSC
SEEKING
COSP
I/O 1
I/O Ø
I/O 11
I/O 10
REG SEL
OSP
7485 F5
74298 F4
7485 D3
74298 E3
74157 E7
7485 F7
74175 F6
7402 G2
7408 E1
7404 H1
7438 B3
7438 B3
7438 A3
7438 A3
7438 A3
7438 A2
PC
F1-9 SHT.5
TA5
TA4
TA3
TA2
TA1
TAØ
SA3
SA2
SC
SA1
SAØ
2-21
2-19
E2-13 SHT.5
E2-12 SHT 5
F2-4 SHT 5
F2-3 SHT.6
2-17
2-15
2-13
2-11
F2-2, SHT.5
F2-1, SHT.6
F2-15, SHT.5
F2-14, SHT.5
G6-2, SHT.6
F2-13, SHT.5
F2-12, SHT.5
A2-9 SHT.4
A2-4 SHT.4
A2-10 SHT.4
A2-1 SHT.4
+5V


SCALE: NONE
DATE 4-29-74
APPROVED BY
DRAWN: R S
FLOPPY FORMATTER
SHT 4 OF 8
DRAWING NO 101024-E
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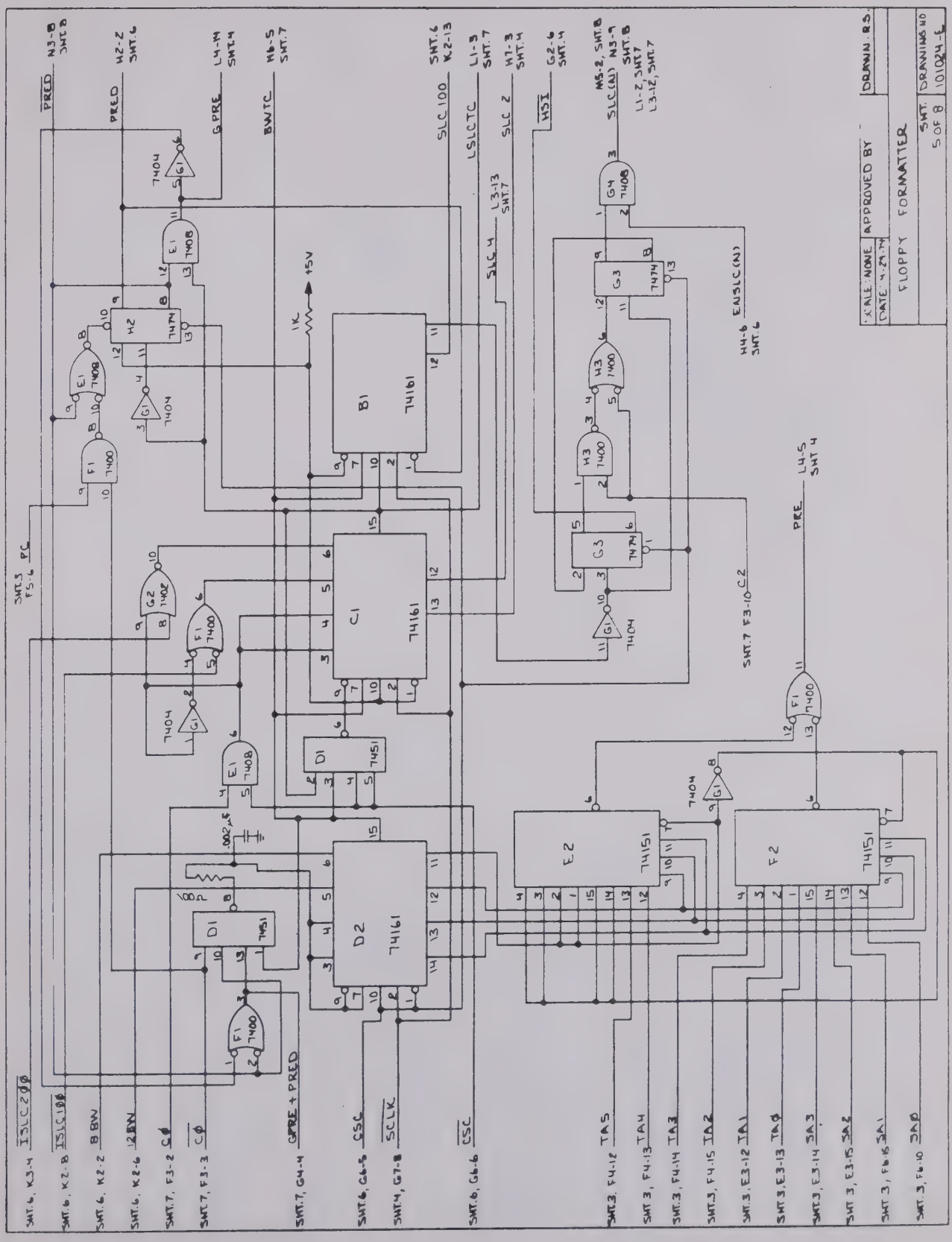
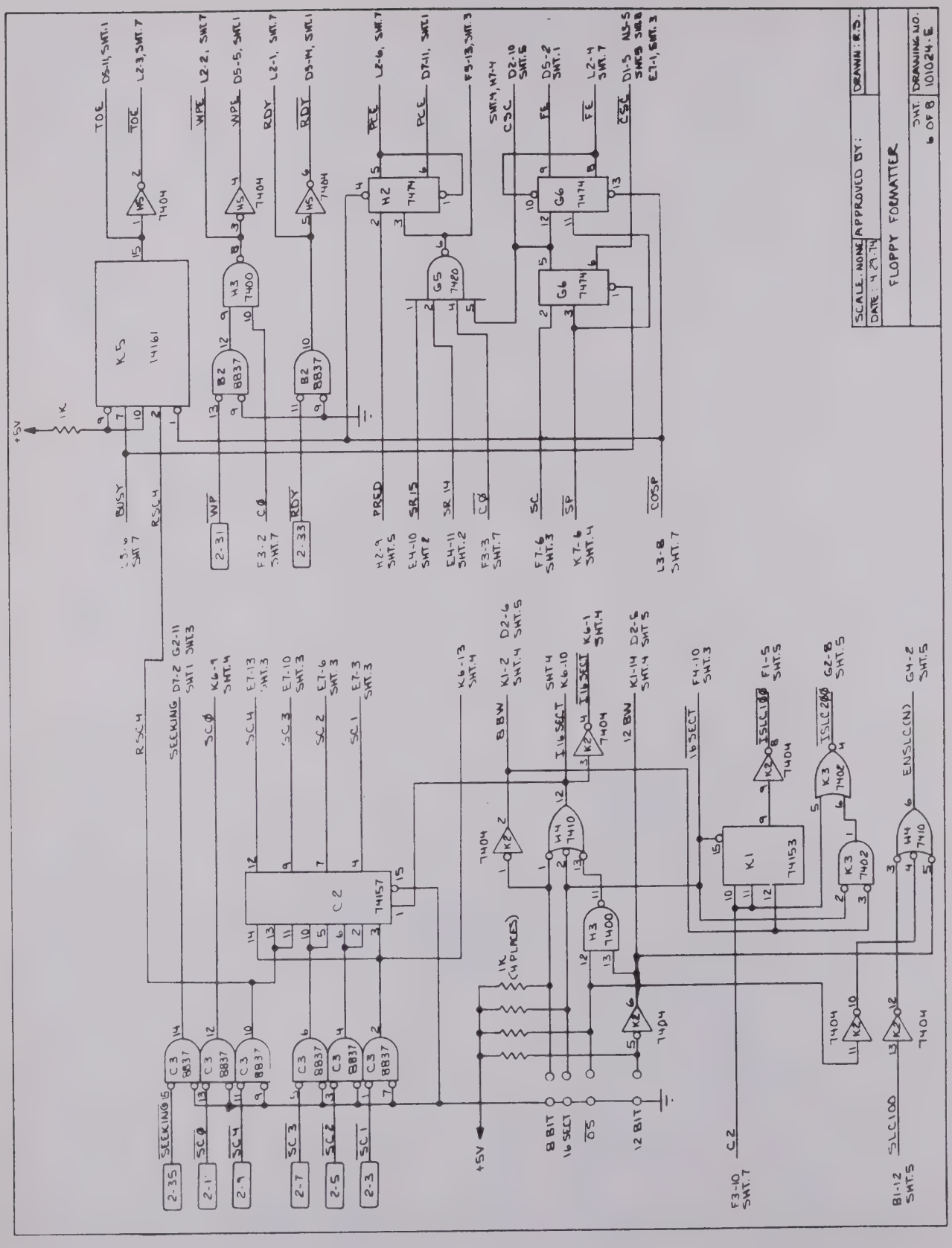
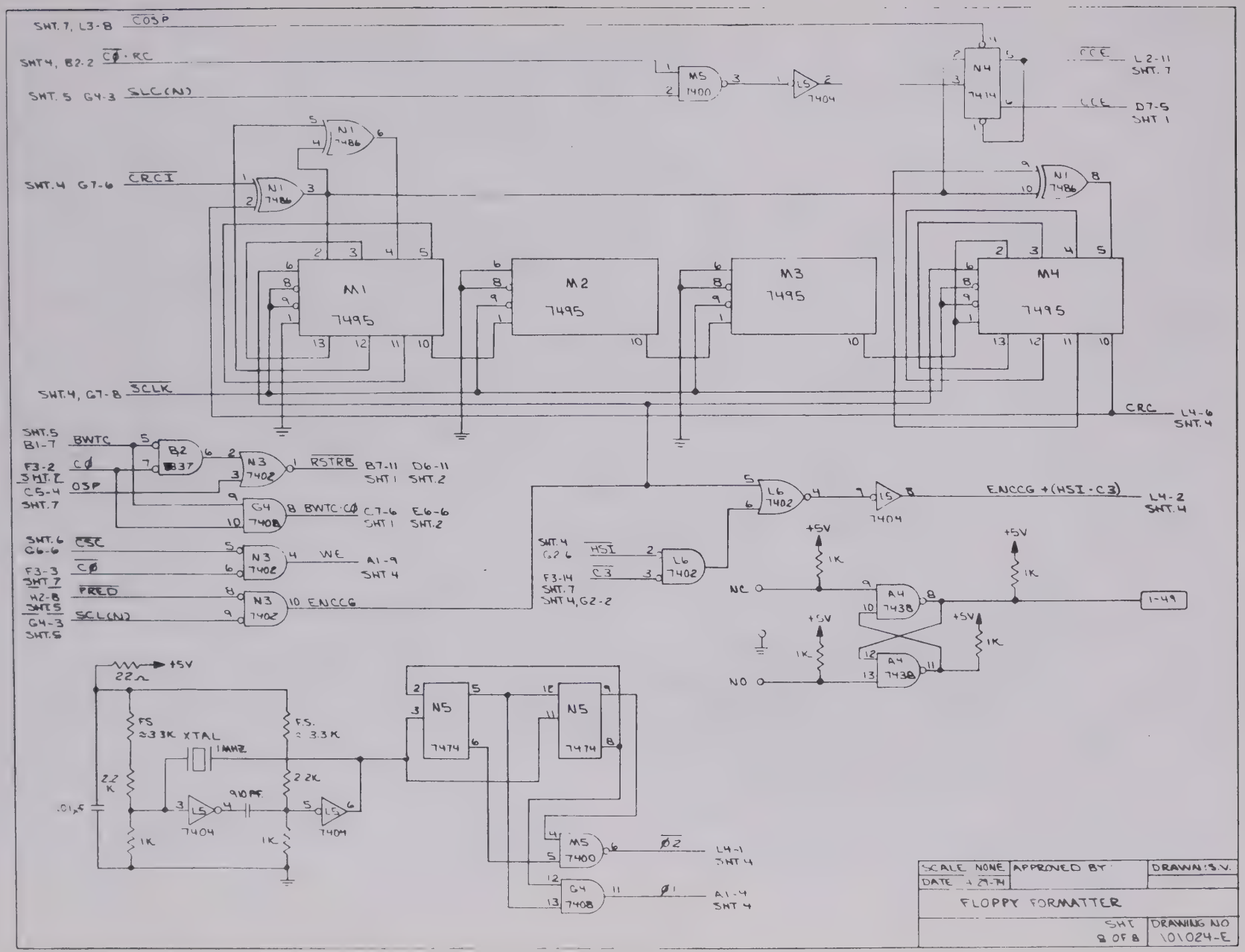
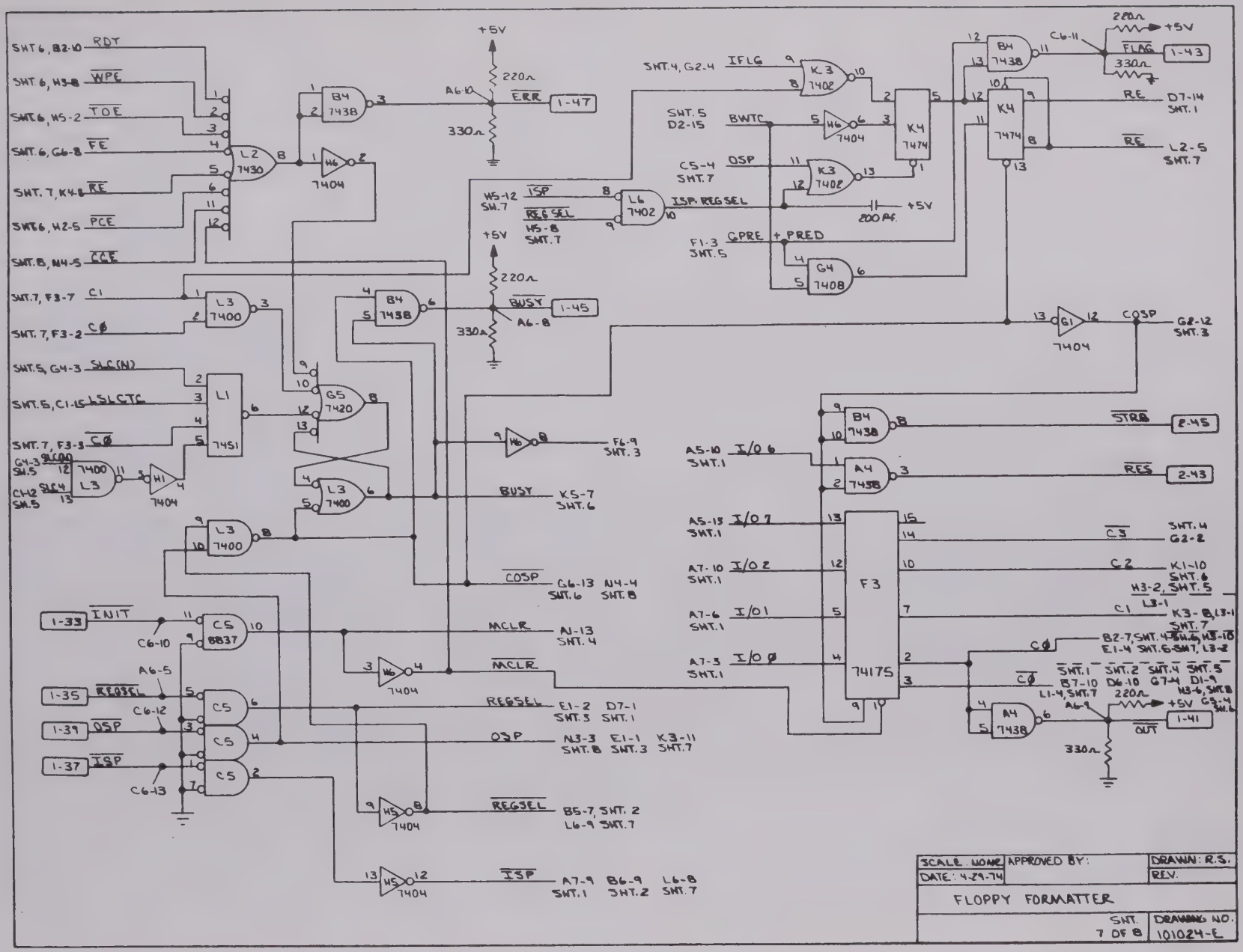
SHT.3, F6-2 UØ
SHT.3, F6-6 U1
SHT.3, F6-3 UØ
SHT 7 C5-10 MCLR
SHT 8, N3-4 WE
SHT.8 G4-11 Ø1
SHT.2, E4-10 SR15
SHT.2, F6 10 SR11
SHT 1 D4-10 SR7
MT.6, K2-2 8 BW
NT.6, K2-6 12 BW
SHT 5, F1-11 PRE
SHT.8, L5-8 ENCCG+(HSI·C3)
SHT 5, E1-11 GPRE
SHT.8, M5-6 Ø2
2-39 DATA
2-37 RC
SHT 7, F3-2 CØ
SHT 7, F3-3 CØ
SHT 8 M4-10 CRC
SHT 6 C3-12 CØ
SHT 6, H4-12 I·6 SECT
SHT 6, C3-2 SC1
SHT 6, K2-4 I·6 SECT
SHT 5 G3-6 HSI
SHT 4 G6-5 CSC
SHT 5, C1-13 SCC 2
SHT 7 F3-14 CS
7438 A2
7438 A1
7428 A1
D3 2-29
D2 2-27
D1 2-25
DØ 2-23
MCLR 2-47
WE 2-41
DATA 2-39
74163 K1
74153 L4
8837 B2
7404 H1
7474 H7
7451 G7
7451 K6
9601 K7
7402 G2
1K
+5V
200 PF
5.1K
SCLK
C7-8 SHT 1
E6-8 SHT 2
D2-2, SHT 5
M1-9 SHT 8
CRC I
N1-1, SHT 8
RD
C7-1, SHT 1
CØ · RC
M5-1, SHT 8
SP
G6 3 SHT 6
IFLG
K3-9 SHT 7

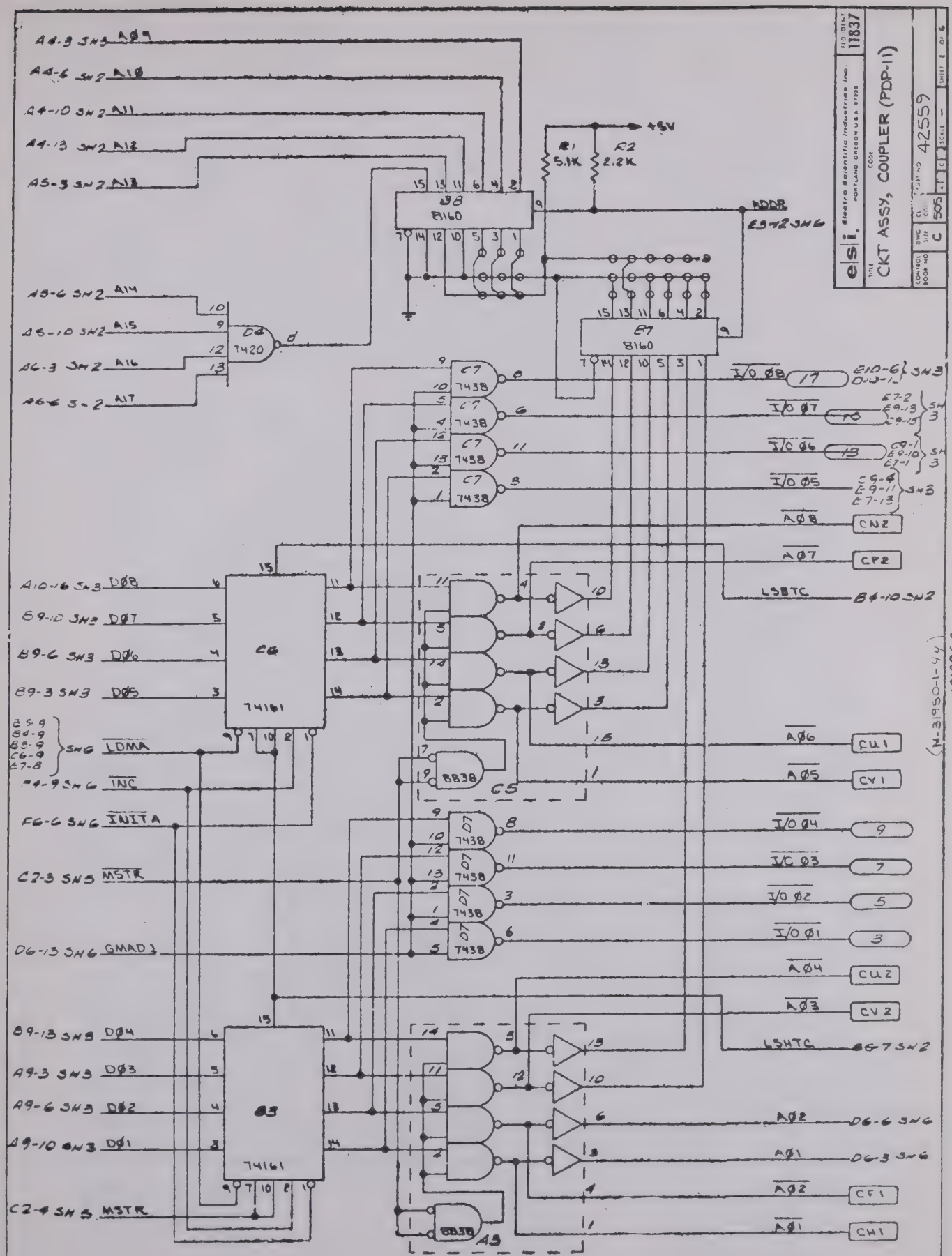

FLOPPY FORMATTER
DRAWN B.S.
APPROVED BY
DRAWING NO 1010246
SHT. 5 OF 8
SCALE: NONE
DATE: 4-29-77
B1 74161
C1 74161
D2 74161
E2 74151
F2 74151
D1 74151
+5V
1K
.002μF
68Ω
PRED
GPRE
BWTC
SLC 100
LSLCTC
SLC 4
SLC 2
HSI
ENSLC(N)
PRE
TAS
TA4
TA3
TA2
TA1
TA0
SA3
SA2
SA1
SA0
CSC
SCLK
C2
C0

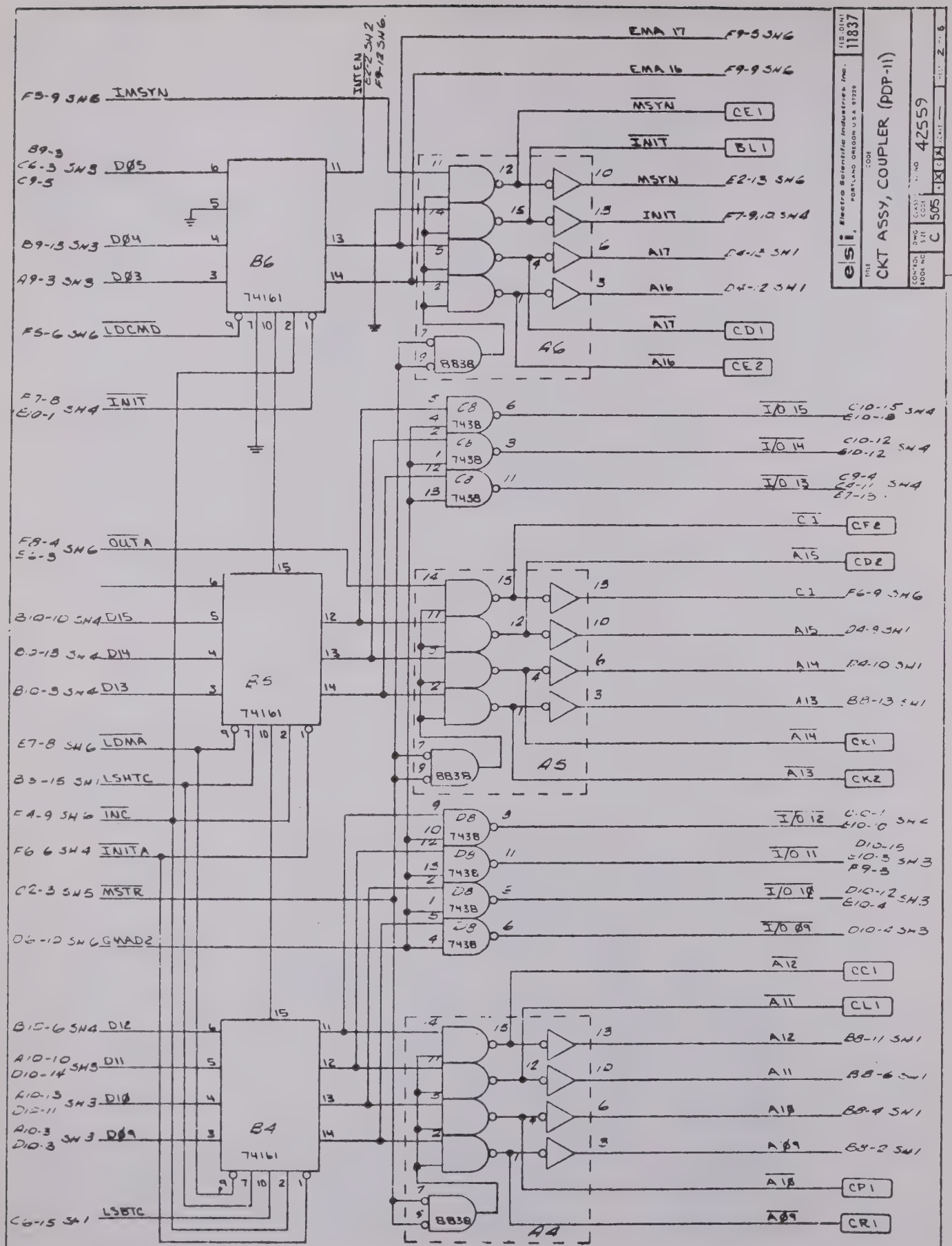

SCALE: NONE
APPROVED BY:
DRAWN: R.D.
DATE: 4-29-74
FLOPPY FORMATTER
SHT. 6 OF 8
DRAWING NO. 101024-E
K5 74161
C2 74157
K1 74153
K2 7404
K3 7402
H3 7400
H4 7410
G5 7420
H2 7474
G6 7474
B2 8837
C3 8837
+5V
1K
1K (4 PLACES)
BUSY
RSC4
SEEKING
SC0
SC4
SC3
SC2
SC1
WP
C0
RDY
PRSD
SR15
SR14
C0
SC
SP
COSP
TOE
WPE
RDY
PCE
C3C
FE
CSC
8 BIT
16 SECT
DS
12 BIT
C2
SLC100
ENSLC(N)
TSLC100
TSLC200

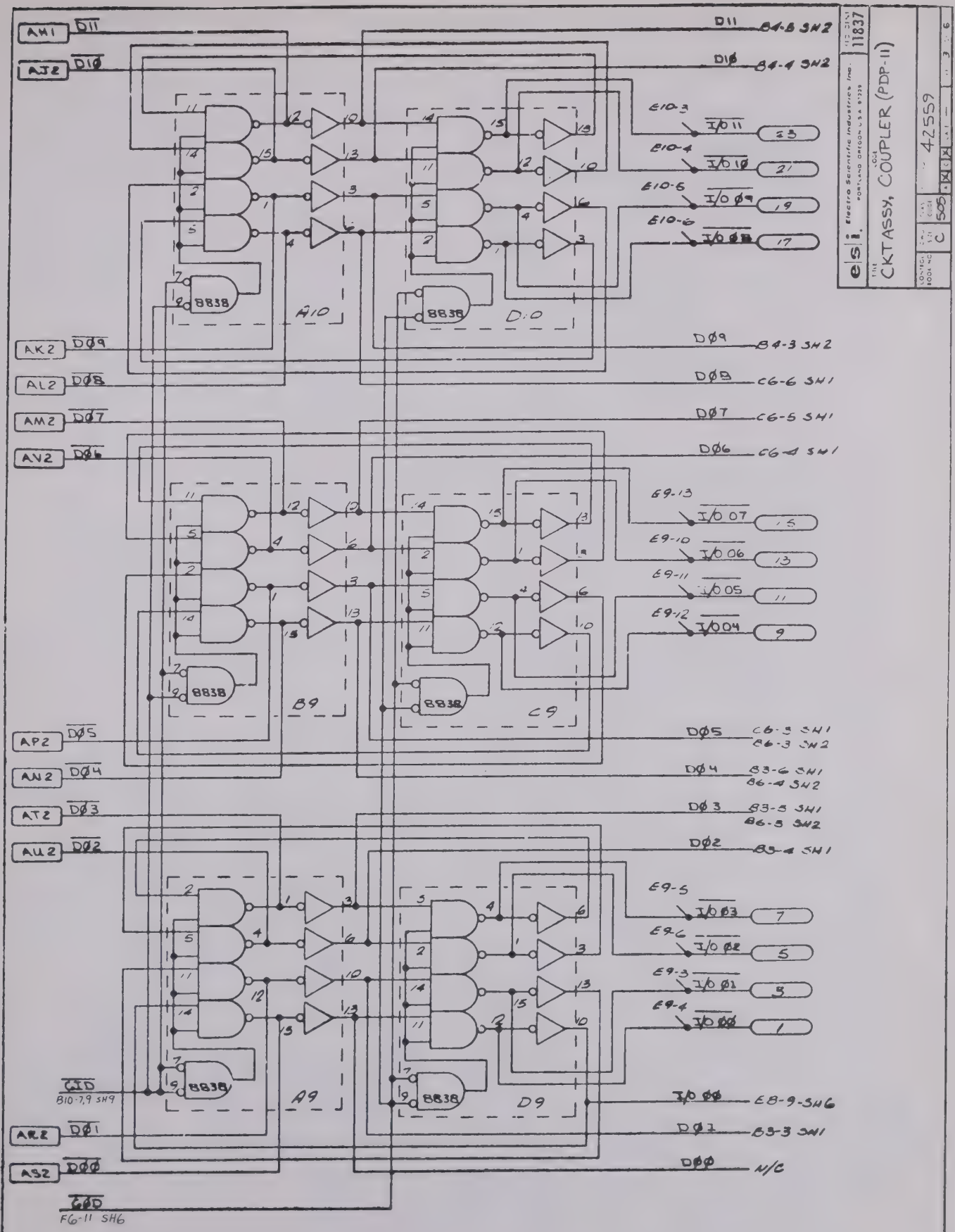


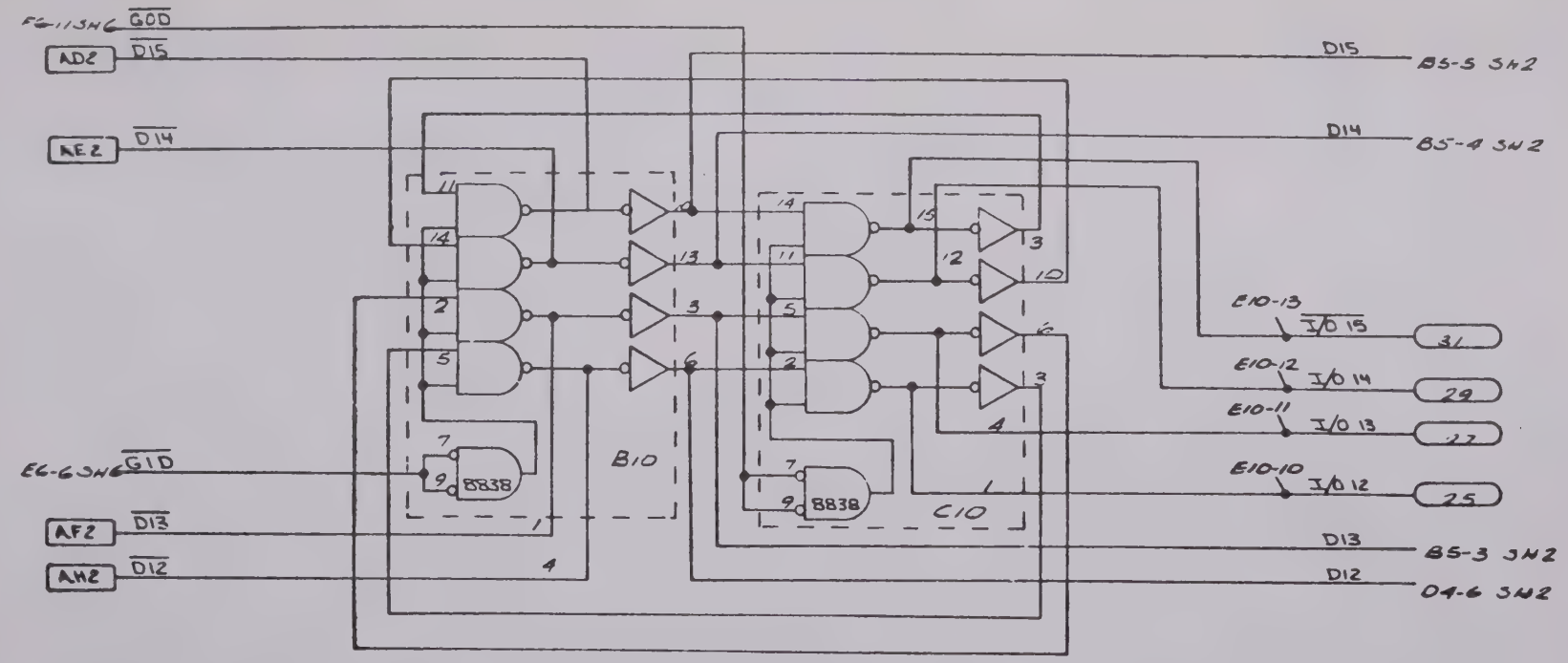
SCALE NONE	APPROVED BY	DRAWN S.V.
DATE 4-29-74		
FLOPPY FORMATTER		
SHT 8 OF 8	DRAWING NO 101024-E	

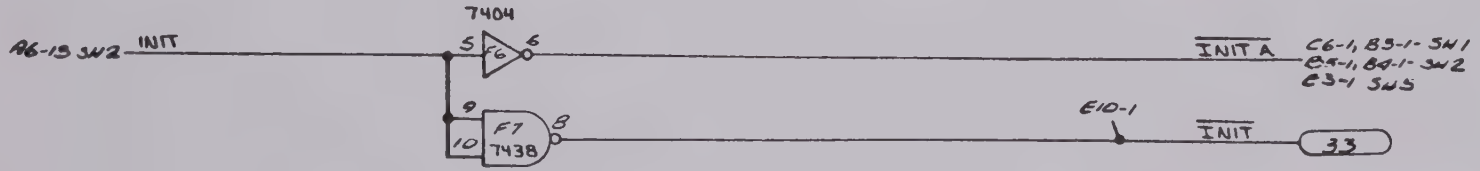

SHT.6, B2-10 RDY
SHT.6, H3-8 WPE
SHT.6, H5-2 TOE
SHT.6, G6-8 FE
SHT.7, K4-8 RE
SHT.6, H2-5 PCE
SHT.8, N4-5 CCE
SHT.7, F3-7 C1
SHT.7, F3-2 CØ
SHT.5, G4-3 SLC(N)
SHT.5, C1-6 LSLCTC
SHT.7, F3-3 CØ
G4-3 SW.5 SLC4
CH2 SW.5 SLC4
+5V
220Ω
A6-10
330Ω
ERR
1-47
BUSY
1-45
A6-8
ISP
REGSEL
H5-12 SW.7
H5-8 SHT.7
200 Pf.
IFLG
SHT.4, G2-4
BWTC
SHT.5 D2-15
DSP
C5-4 SHT.7
GPRE
F1-3 SHT.5
+PRED
C6-11
FLAG
1-43
RE
D7-14 SHT.1
L2-5 SHT.7
COSP
G2-12 SHT.3
F6-9 SHT.3
BUSY
K5-7 SHT.6
COSP
G6-13 N4-4 SHT.6 SHT.8
INIT
1-33
C6-10
MCLR
N1-13 SHT.4
A6-5
REGSEL
1-35
C6-12
DSP
1-39
ISP
1-37
C6-13
REGSEL
B5-7, SHT.2 L6-9 SHT.7
ISP
A7-9 B6-9 L6-8 SHT.1 SHT.2 SHT.7
A5-10 I/O 6
A5-15 I/O 7
A7-10 I/O 2
A7-6 I/O 1
A7-3 I/O Ø
F3
74175
STRB
E-45
RES
2-43
C3
SHT.4 G2-2
C2
K1-10 SHT.6
H3-2, SHT.5 L3-1
C1
K3-8, L3-1 SHT.7
CØ
B2-7, SHT.4 SW.6, H3-10 E1-4 SHT.6 SHT.7, L3-2
SHT.1 SHT.2 SHT.4 SHT.5 B7-10 D6-10 G7-4 D1-9 L1-4, SHT.7 H3-6, SHT.8 A6-9
220Ω
+5V
C9-4 SW.6
OUT
1-41
330Ω
SCALE: NONE
APPROVED BY:
DRAWN: R.S.
DATE: 4-29-74
REV.
FLOPPY FORMATTER
SHT. 7 OF 8
DRAWING NO. 101024-E

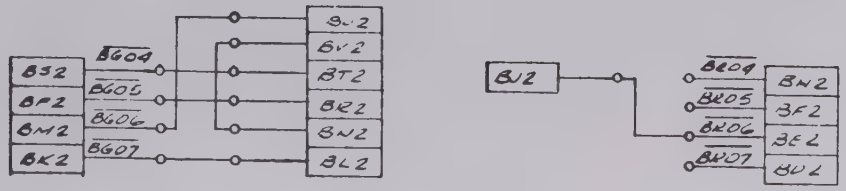

e|s|i Electro Scientific Industries Inc. PORTLAND OREGON U.S.A. 97229
FID:DIAT 11837
TITLE CKT ASSY, COUPLER (PDP-11)
CODE IDENT NO 42559
DWG SIZE C
SCALE —
SHEET 1 OF 6
CONTROL BOOK NO
+5V
R1 5.1K
R2 2.2K
ADDR
E3-12 SN6
E8 8160
E7 8160
D8 7420
C7 7438
C6 74161
C5 8838
B3 74161
A3 8838
A4-9 SN3 AØ9
A4-6 SN3 A10
A4-10 SN2 A11
A4-13 SN2 A12
A5-3 SN2 A13
A5-6 SN2 A14
A5-10 SN2 A15
A6-3 SN2 A16
A6-6 S-2 A17
I/O ØB
I/O Ø7
I/O Ø6
I/O Ø5
AØ8
AØ7
LSBTC
B4-10 SN2
A10-16 SN3 DØ8
B9-10 SN3 DØ7
B9-6 SN3 DØ6
B9-3 SN3 DØ5
LDMA
INC
INITA
MSTR
GMAD
B9-13 SN3 DØ4
A9-3 SN3 DØ3
A9-6 SN3 DØ2
A9-10 SN3 DØ1
AØ6
AØ5
I/O Ø4
I/O Ø3
I/O Ø2
I/O Ø1
AØ4
AØ3
LSHTC
B6-7 SN2
AØ2
AØ1
D6-6 SN6
D6-3 SN6
CU1
CV1
CU2
CV2
CF1
CH1
X1010960
(M-31950-1-44)


CKT ASSY, COUPLER (PDP-11)
esi
Electro Scientific Industries Inc.
PORTLAND OREGON U.S.A. 97229
11837
42559
C
505
IMSYN
DØ5
DØ4
DØ3
LDCMD
INIT
OUT A
D15
D14
D13
LDMA
LSHTC
INC
INITA
MSTR
D12
D11
D10
DØ9
LSBTC
B6
74161
B5
74161
B4
74161
A6
A5
A4
8838
7438
EMA 17
EMA 16
MSTN
INIT
A17
A16
A15
A14
A13
A12
A11
A10
A09
I/O 15
I/O 14
I/O 13
I/O 12
I/O 11
I/O 10
I/O 09
C1
CE1
BL1
CD1
CE2
CF2
CD2
CK1
CK2
CC1
CL1
CP1
CR1

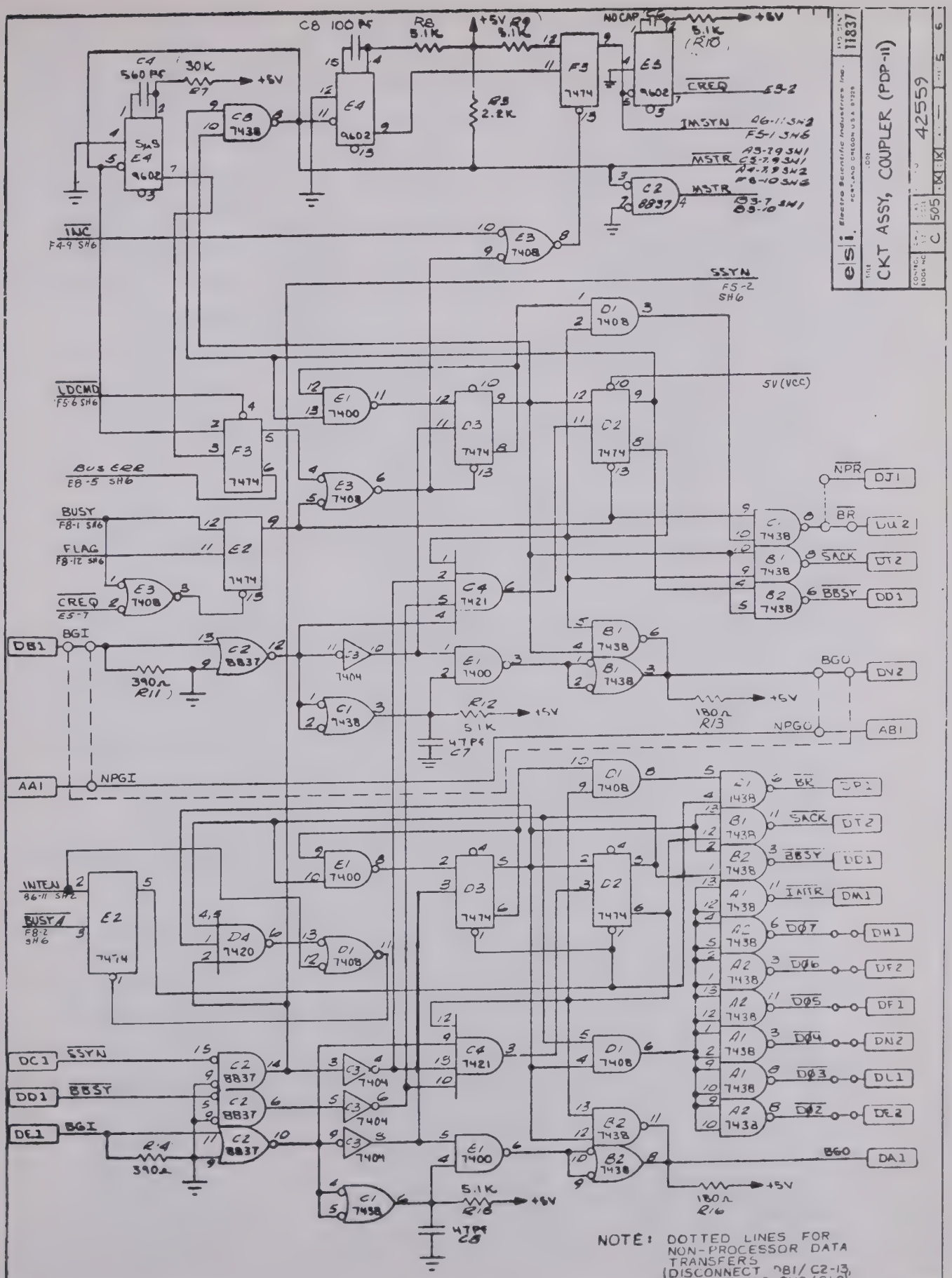

AH1 D11
AJ2 D10
AK2 DØ9
AL2 DØ8
AM2 DØ7
AV2 DØ6
AP2 DØ5
AN2 DØ4
AT2 DØ3
AU2 DØ2
AR2 DØ1
AS2 DØØ
CID
B10-7,9 SH9
CDD
FG-11 SH6
A10
D10
B9
C9
A9
D9
8838
D11 B4-8 SH2
D10 B4-1 SH2
DØ9 B4-3 SH2
DØ8 C6-6 SH1
DØ7 C6-5 SH1
DØ6 C6-4 SH1
DØ5 C6-3 SH1
B6-3 SH2
DØ4 B3-6 SH1
B6-4 SH2
DØ3 B3-5 SH1
B6-5 SH2
DØ2 B3-4 SH1
DØ1 B3-3 SH1
DØØ N/C
E10-3 I/O 11 23
E10-4 I/O 10 21
E10-5 I/O Ø9 19
E10-6 I/O ØB 17
E9-13 I/O 07 15
E9-10 I/O 06 13
E9-11 I/O 05 11
E9-12 I/O 04 9
E9-5 I/O Ø3 7
E9-6 I/O Ø2 5
E9-3 I/O Ø1 3
E9-4 I/O ØØ 1
I/O ØØ E8-9-SH6
11837
CKTASSY, COUPLER (PDP-11)
42559
C
505

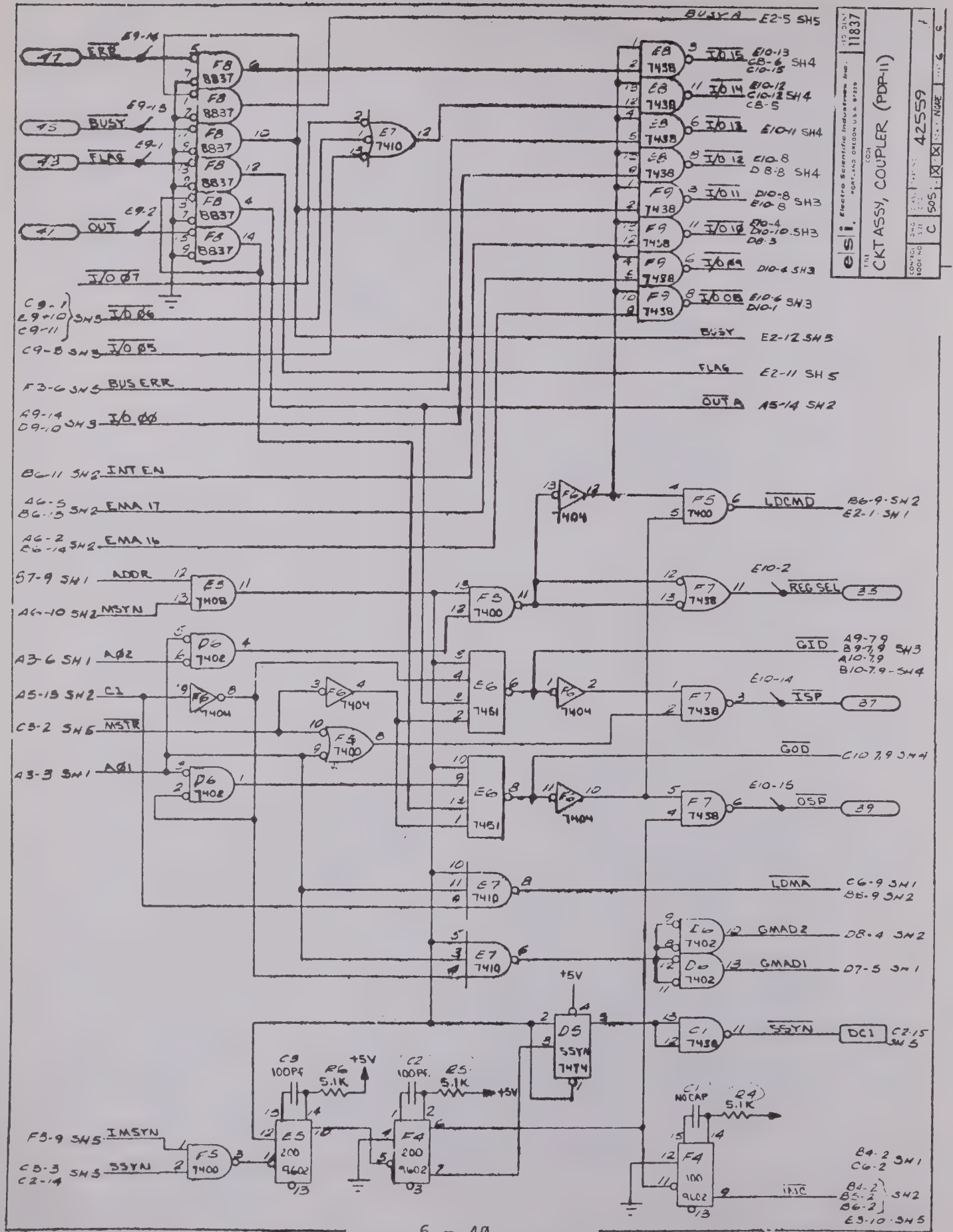


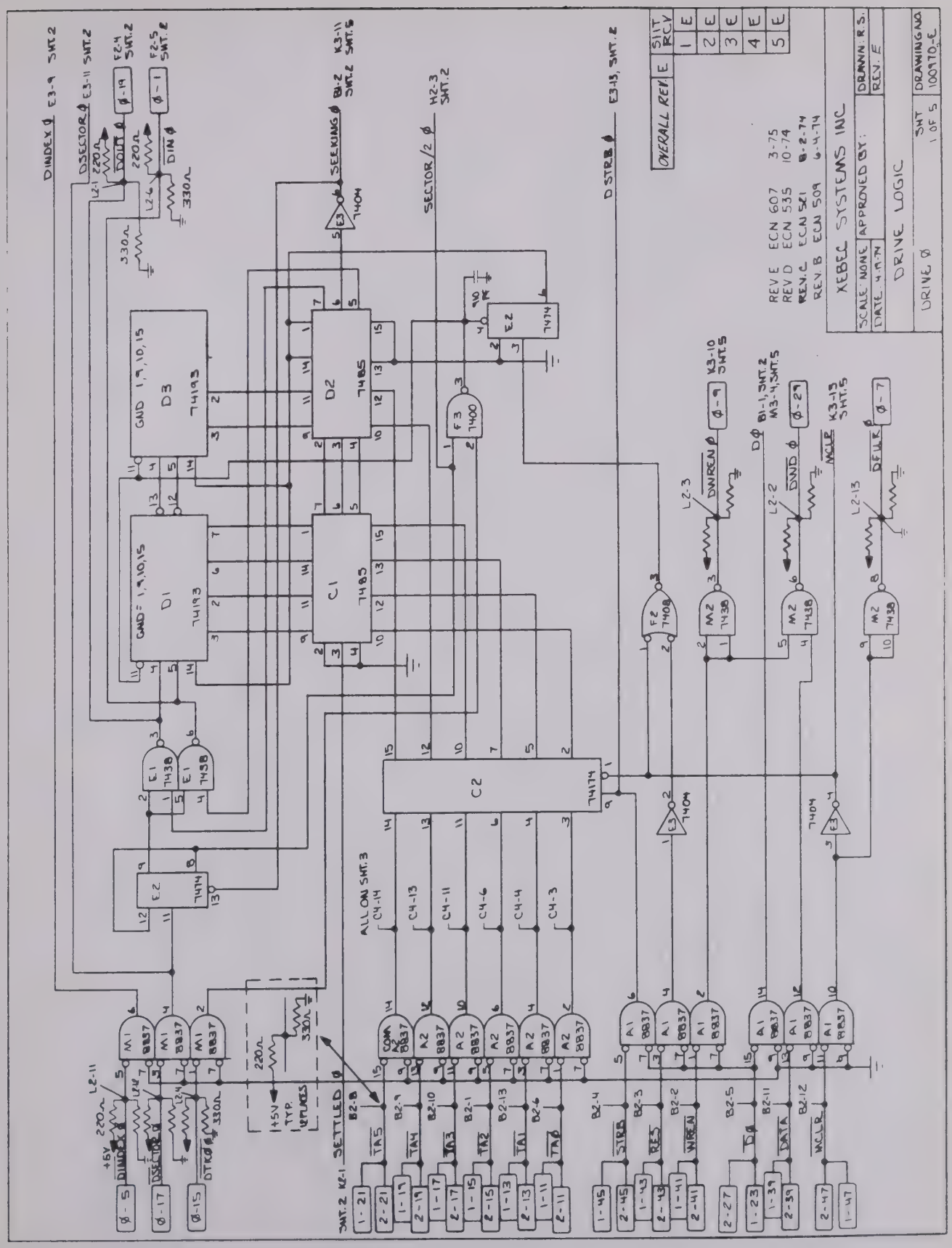


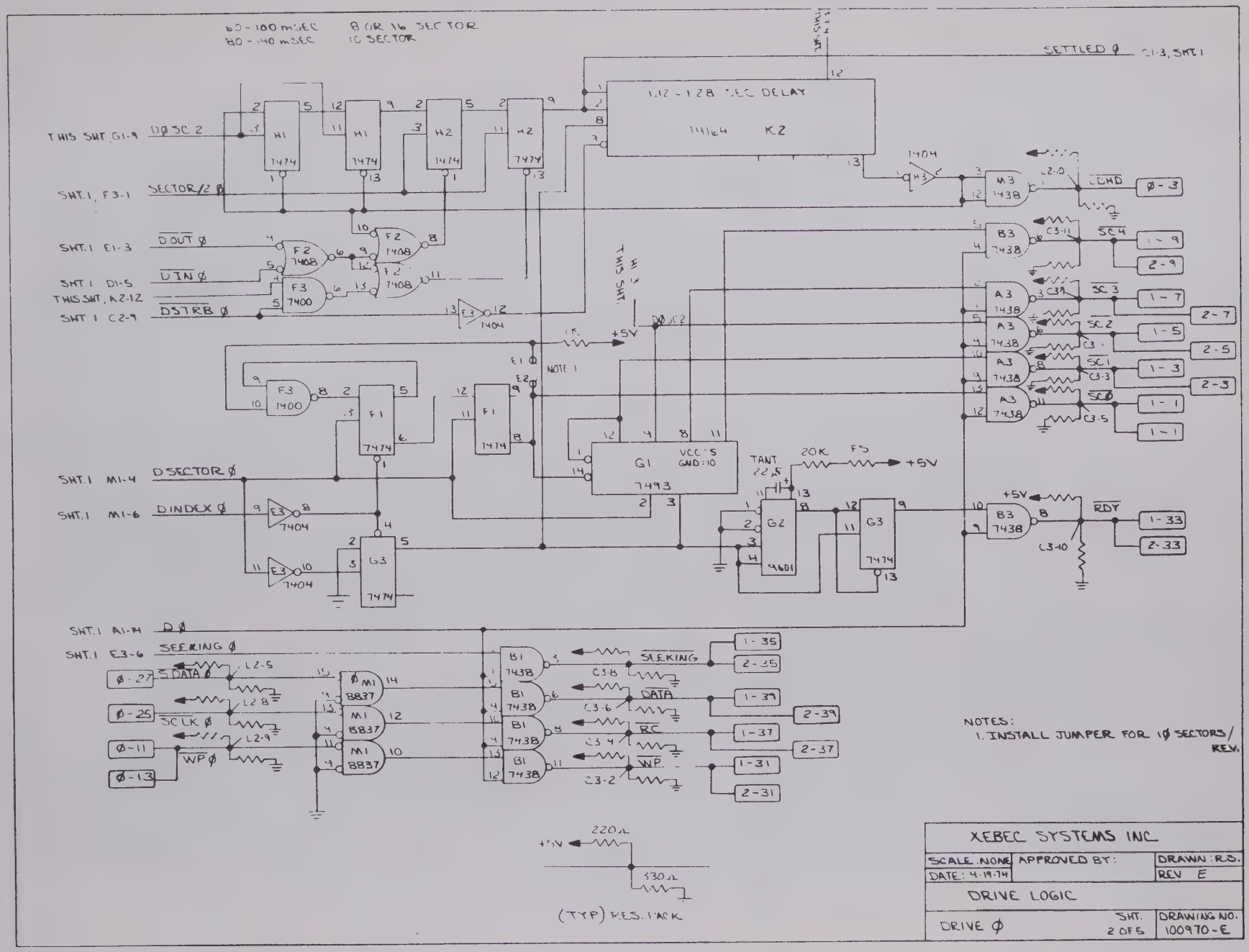


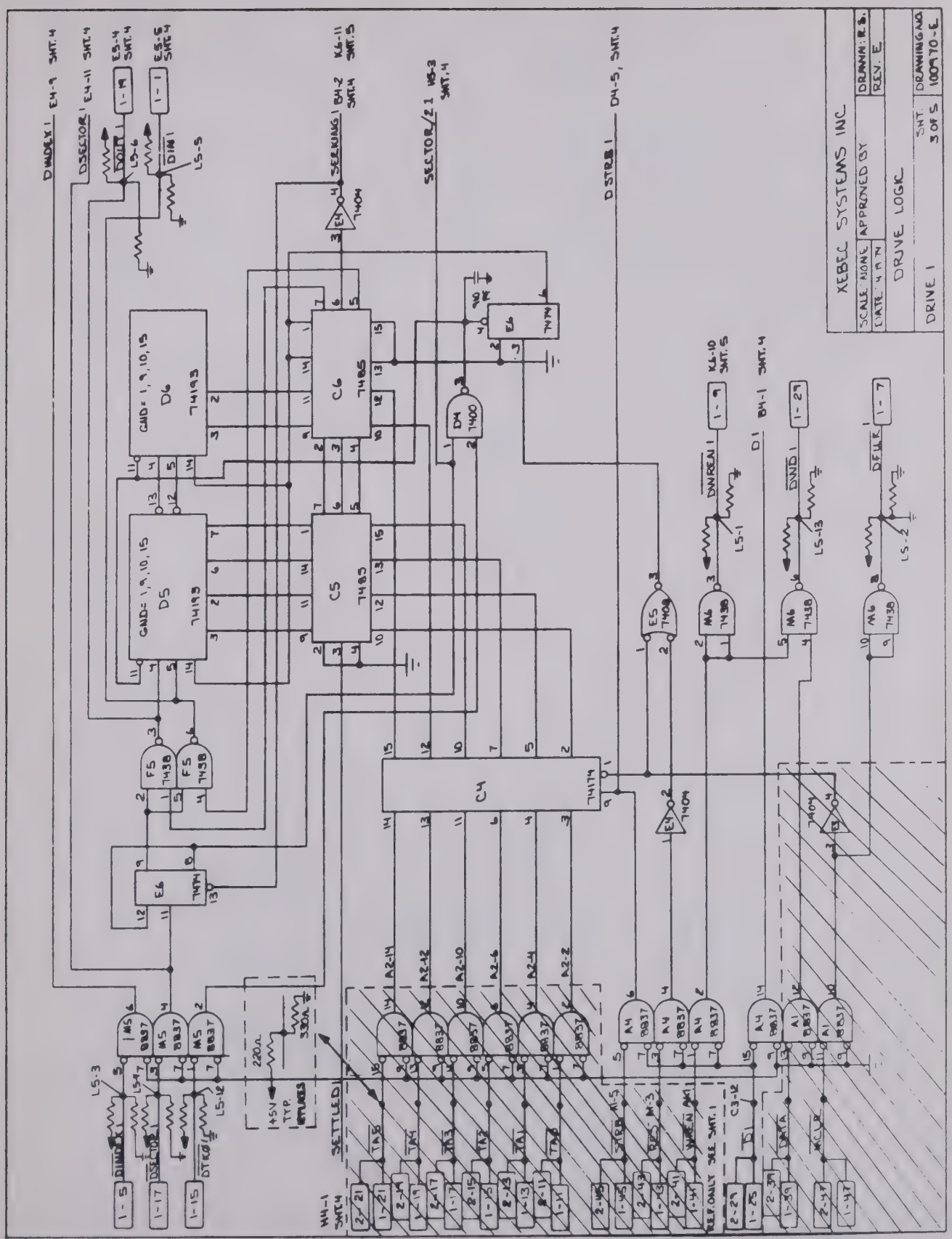
esi. Electro Scientific Industries Inc. PORTLAND OREGON U.S.A. 97229				REVISION 11837
TITLE CKT ASSY, COUPLER (PDP-11)				CODE
CONTROL BOOK NO	DWG SIZE C	CLASS CODE 505	DWG NO 42559	SCALE —

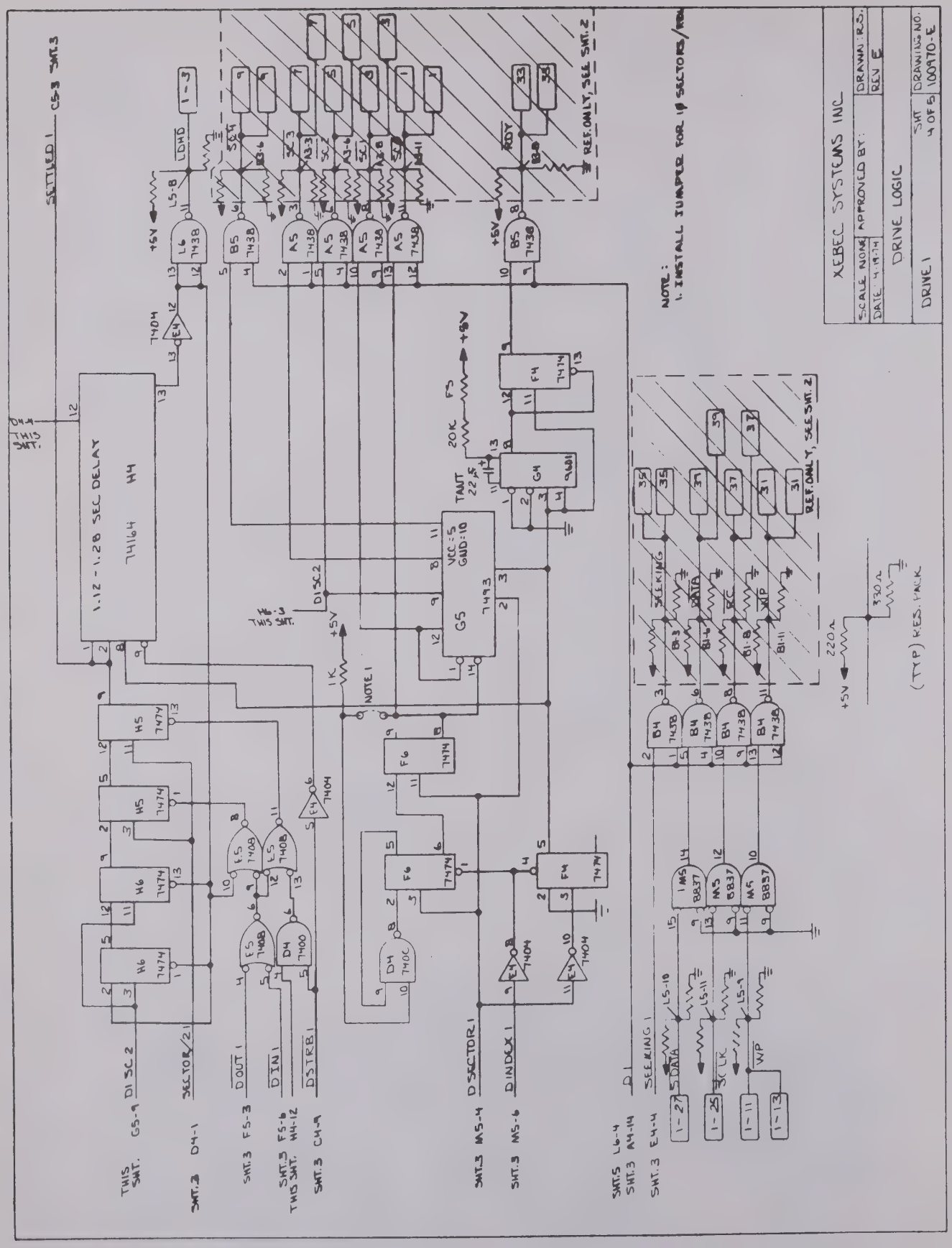

C8 100 PF
RB 5.1K
+5V
RA 5.1K
NO CAP
5.1K (R10)
+5V
C4 560 PF
30K
R7
+5V
C8 7438
E4 9602
F3 7474
E5 9602
CREQ
ES-2
RB 2.2K
IMSYN
MSTR
C2 8837
INC
F4-9 SH6
E3 7408
SSYN
FS-2 SH6
D1 7408
LDCMD
FS-6 SH6
E1 7400
D3 7474
C2 7474
5V (VCC)
F3 7474
BUS ERR
EB-5 SH6
BUSY
FB-1 SH6
FLAG
FB-12 SH6
CREQ
ES-7
E2 7474
C4 7421
NPR
DJ1
BR
DU2
SACK
DT2
BBSY
DD1
DB1
BGI
C2 8837
390Ω R11
C3 7404
B1 7438
B2 7438
BGO
DV2
R12 5.1K
+5V
180Ω R13
NPGO
AB1
47 PF C7
AA1
NPGI
C1 7438
A1 7438
A2 7438
INTEN
B6-11 SH2
BUSY A
FB-2 SH6
D4 7420
DC1
DD1
DE1
R14 390Ω
R16 180Ω
DA1
5.1K R18
47PF C8
NOTE: DOTTED LINES FOR NON-PROCESSOR DATA TRANSFERS (DISCONNECT DB1/C2-13, DV2/B1-3 AND DU2/C1-9)
DWG NO 11837
esi Electro Scientific Industries Inc. PORTLAND OREGON U.S.A. 97229
TITLE CKT ASSY, COUPLER (PDP-11)
DWG NO 42559
CONTRACT NO
BOOK NO
C
505

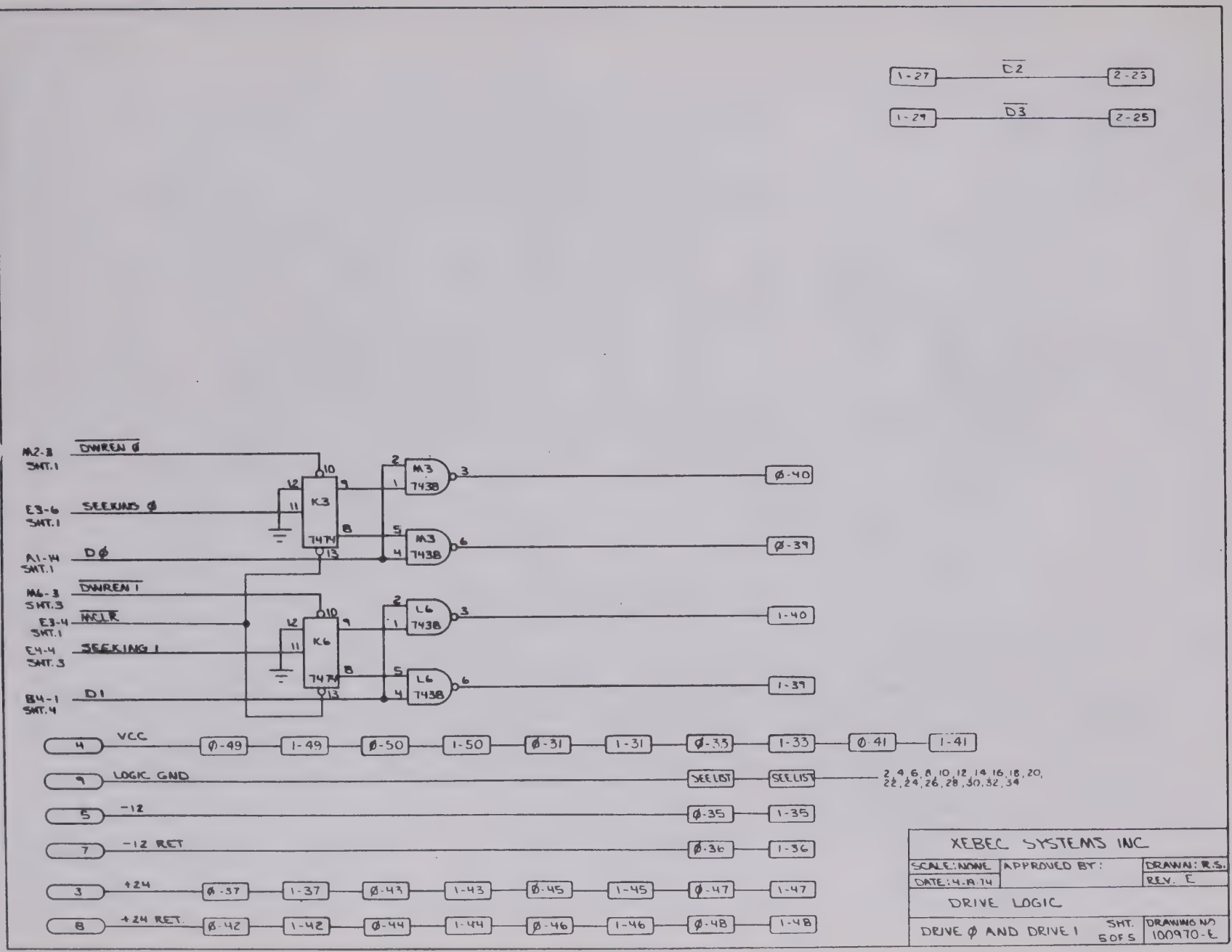

CKT ASSY, COUPLER (PDP-11)
esi. Electro Scientific Industries Inc. PORTLAND OREGON U.S.A. 97220
11837
42559
C
505
ERR
BUSY
FLAG
OUT
I/O Ø7
I/O Ø6
I/O Ø5
BUS ERR
I/O ØØ
INT EN
EMA 17
EMA 16
ADDR
MSYN
AØ2
C1
MSTR
AØ1
IMSYN
SSYN
LDCMD
REG SEL
GID
ISP
GOD
OSP
LDMA
GMAD2
GMAD1
SSYN
IAIC
BUSY A
OUT A
+5V
100PF
5.1K
NOCAP

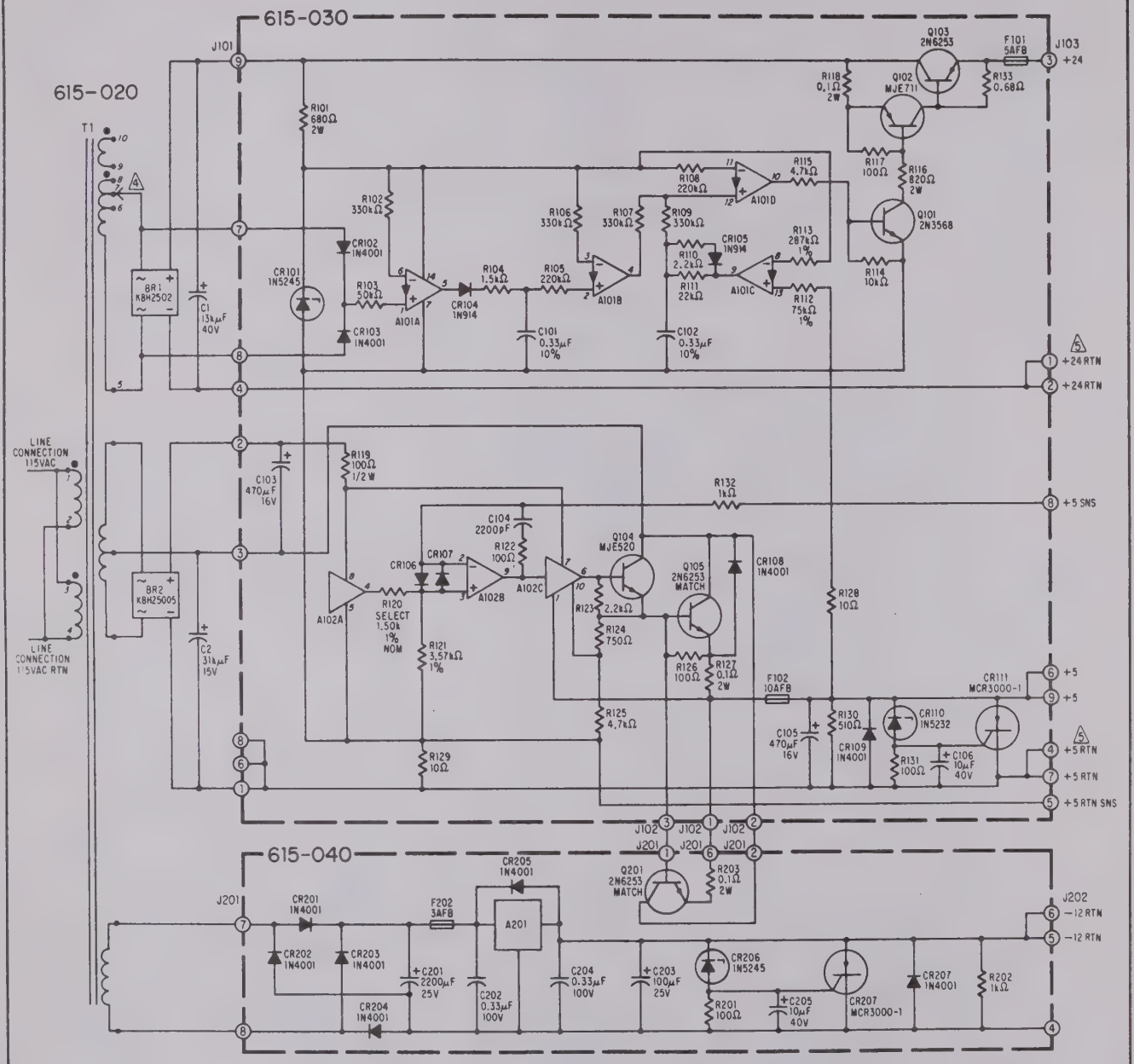

XEBEC SYSTEMS INC
DRIVE LOGIC
DRIVE Ø
SCALE: NONE
DATE: 4-19-74
APPROVED BY:
DRAWN: R.S.
REV. E
DRAWING NO. 100170-E
SHT 1 OF 5
OVERALL REV E
REV E ECN 607 3-75
REV D ECN 535 10-74
REV C ECN 501 8-2-74
REV B ECN 509 6-4-74
DINDEX Ø E3-9 SHT.2
DSECTOR Ø E3-11 SHT.2
DOUT Ø
DIN Ø
SEEKING Ø B4-2 K3-11 SHT.2 SHT.5
SECTOR/2 Ø H2-3 SHT.2
DSTRB Ø E3-13, SHT.2
DWREN Ø K3-10 SHT.5
DWND Ø B1-1, SHT.2 M3-4, SHT.5
MCLR K3-13 SHT.5
DFLT Ø
ALL ON SHT.3
SHT.2 K2-1 SETTLED Ø
+5V TYP. 4 PLACES
D1
D2
D3
C1
C2
E1
E2
E3
F2
F3
M1
M2
A1
A2
74193
7485
74174
7438
8837
7404
7400
7474


60 - 100 m SEC 8 OR 16 SECTOR
80 - 140 m SEC 10 SECTOR
SETTLED Ø
1.12 - 128 SEC DELAY
74164 K2
THIS SHT G1-9 DØ SC 2
SHT. 1, F3-1 SECTOR/2 Ø
SHT.1 E1-3 DOUT Ø
SHT 1 D1-5 DIN Ø
THIS SHT. A2-12
SHT 1 C2-9 DSTRB Ø
SHT.1 M1-4 DSECTOR Ø
SHT.1 M1-6 DINDEX Ø
SHT.1 A1-H DØ
SHT.1 E3-6 SEEKING Ø
Ø-27 SDATA Ø
Ø-25 SCLK Ø
Ø-11 WP Ø
Ø-13
+5V
TANT 22 µF
20K
NOTE 1
E1 Ø
E2 Ø
SEEKING
DATA
RC
WP
SC 4
SC 3
SC 2
SC 1
SC Ø
RDY
220Ω
330Ω
(TYP) RES. PACK
NOTES:
1. INSTALL JUMPER FOR 1Ø SECTORS/
REV.
XEBEC SYSTEMS INC.
SCALE: NONE
APPROVED BY:
DRAWN: R.S.
DATE: 4-19-74
REV E
DRIVE LOGIC
DRIVE Ø
SHT. 2 OF 5
DRAWING NO. 100970-E


XEBEC SYSTEMS INC
SCALE: NONE
APPROVED BY
DRAWN: R.B.
DATE: 4-7-7
REV. E
DRIVE LOGIC
DRIVE 1
SHT. 3 OF 5
DRAWING NO. 100970-E
DINDEX
DSECTOR
DOUT
DIN
SEEKING
SECTOR/21
DSTRB
DWREN
DWD
DFLT
SETTLED
DRIVE SEL
STEP
DIR
WRITE
REF. ONLY SEE SHT. 1
DATA
CLK
GND= 1, 9, 10, 15
D6 74193
D5 74193
C6 7485
C5 7485
C4 74174
D4 7400
E6 7474
E5 7408
E4 7404
F5 7438
M6 7438
A4 8837
A1 8837
M5 8837
330Ω
220Ω
+5V TYP.


XEBEC SYSTEMS INC
DRIVE LOGIC
DRIVE 1
DRAWING NO. 100970-E
SHT 4 OF 5
REV E
DRAWN: R.S.
SCALE: NONE
DATE: 4-19-79
APPROVED BY:
NOTE:
1. INSTALL JUMPER FOR 17 SECTORS/TRK
SETTLED 1 — C5-3 SHT.3
1.12 - 1.28 SEC DELAY
74LS164
DISC 2
SECTOR 1
DOUT 1
DIN 1
DSTRB 1
DSECTOR 1
DINDEX 1
SEEKING 1
SDATA
SCLK
WP
1K
20K
22µF
330Ω
220Ω
(TYP) RES. PACK
REF. ONLY, SEE SHT. 2
SEEKING
DATA
CLK
WP
+5V
7404
7438
7474
7493
7400
7408
9601
8837


1-27
D2
2-23
1-29
D3
2-25
M2-8 SHT.1
DWREN Ø
E3-6 SHT.1
SEEKING Ø
A1-4 SHT.1
DØ
M6-3 SHT.3
DWREN 1
E3-4 SHT.1
WCLR
E4-4 SHT.3
SEEKING 1
B4-1 SHT.4
D1
K3
K6
7474
M3 7438
L6 7438
Ø-40
Ø-39
1-40
1-39
4 VCC
Ø-49
1-49
Ø-50
1-50
Ø-31
1-31
Ø-33
1-33
Ø-41
1-41
9 LOGIC GND
SEE LIST
2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34
5 -12
Ø-35
1-35
7 -12 RET
Ø-36
1-36
3 +24
Ø-37
1-37
Ø-43
1-43
Ø-45
1-45
Ø-47
1-47
8 +24 RET
Ø-42
1-42
Ø-44
1-44
Ø-46
1-46
Ø-48
1-48
XEBEC SYSTEMS INC
SCALE: NONE
APPROVED BY:
DRAWN: R.S.
DATE: 4-19-74
REV. E
DRIVE LOGIC
DRIVE Ø AND DRIVE 1
SHT. 5 OF 5
DRAWING NO 100970-E

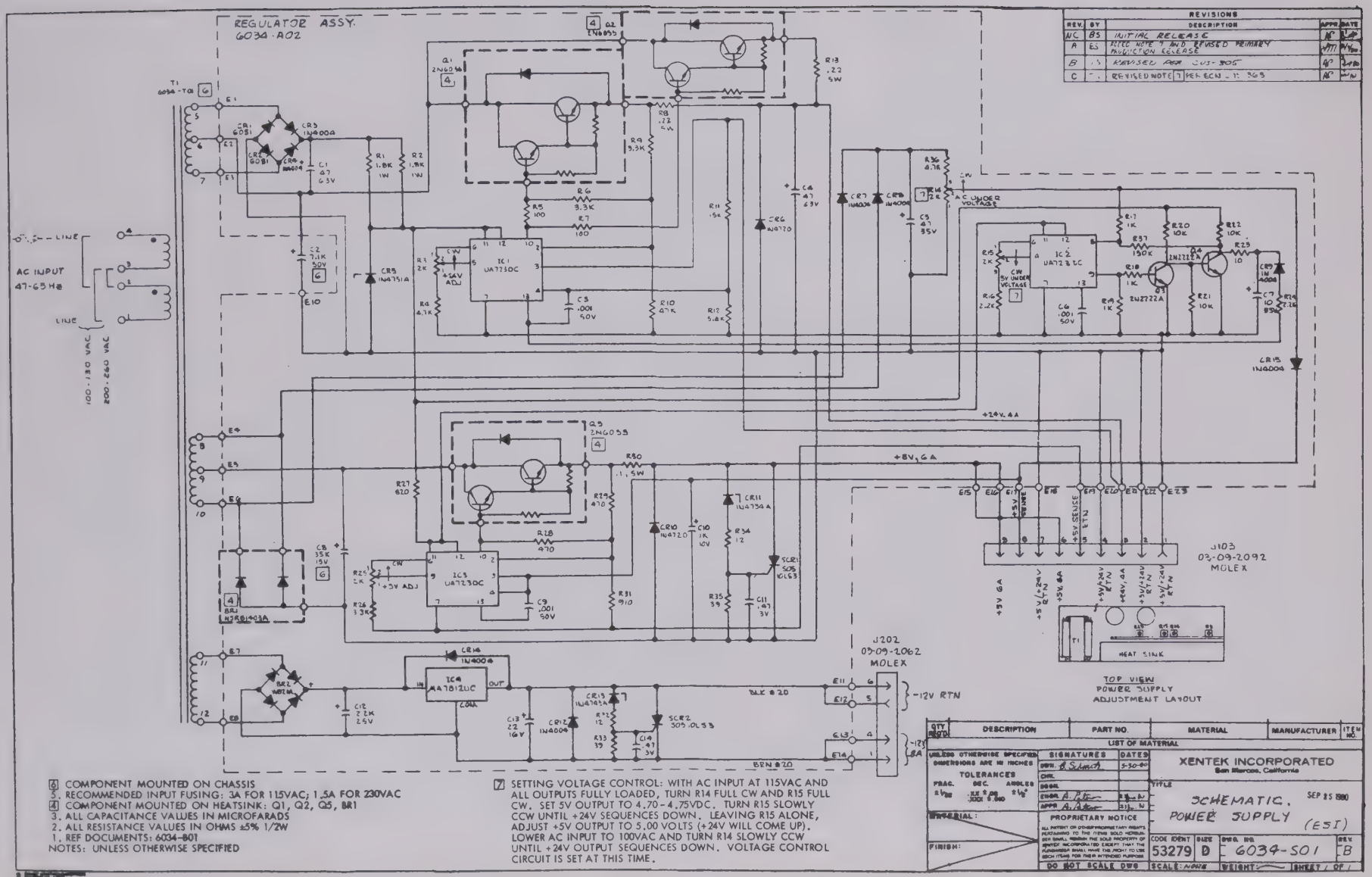


NOTES:

1. A101 = LM3900N, A102 = 723CH, A201 = 7812KC
2. RESISTORS = 5% 1/4W; CAPS = GMV
3. TIE +5SNS TO +5 AND +5RTN SNS TO +5RTN FOR PROPER OPERATION

4. MOVE JUMPER TO OBTAIN PROPER +24. WINDING 9-10 MAY BE USED TO OBTAIN VOLTAGES BETWEEN JUMPER POINTS.
5. +24RTN AND +5RTN MUST BE TIED TOGETHER

DRIVE POWER SUPPLY



[6] COMPONENT MOUNTED ON CHASSIS
5. RECOMMENDED INPUT FUSING: 3A FOR 115VAC; 1.5A FOR 230VAC
[4] COMPONENT MOUNTED ON HEATSINK: Q1, Q2, Q5, BR1
3. ALL CAPACITANCE VALUES IN MICROFARADS
2. ALL RESISTANCE VALUES IN OHMS ±5% 1/2W
1. REF DOCUMENTS: 6034-801
NOTES: UNLESS OTHERWISE SPECIFIED

[7] SETTING VOLTAGE CONTROL: WITH AC INPUT AT 115VAC AND ALL OUTPUTS FULLY LOADED, TURN R14 FULL CW AND R15 FULL CW. SET 5V OUTPUT TO 4.70-4.75VDC. TURN R15 SLOWLY CCW UNTIL +24V SEQUENCES DOWN. LEAVING R15 ALONE, ADJUST +5V OUTPUT TO 5.00 VOLTS (+24V WILL COME UP). LOWER AC INPUT TO 100VAC AND TURN R14 SLOWLY CCW UNTIL +24V OUTPUT SEQUENCES DOWN. VOLTAGE CONTROL CIRCUIT IS SET AT THIS TIME.

LIST OF MATERIAL

QTY REQ'D	DESCRIPTION	PART NO.	MATERIAL	MANUFACTURER	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRAC. ±1/32 DEC. .XX ±.05 .XXX ±.000 ANGLES ±1/2°
MATERIAL:
FINISH:

SIGNATURES	DATES
DSN. R. Schmidt	5-30-80
CHK.	
DRAW. A. Peterson	8-8-80
APPR. A. Peterson	8-11-80

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DO NOT SCALE DWG

XENTEK INCORPORATED
San Marcos, California

TITLE: SCHEMATIC, POWER SUPPLY (ESI)
SEP 25 1980

CODE IDENT 53279 | SIZE D | DWG. NO. 6034-501 | REV. B
SCALE: NONE | WEIGHT: | SHEET 1 OF 1

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Attention: Literature Department

esi Part No. 1872A 6/78

- applications data
- technical articles
- engineering bulletins

☐ EB10 Effects of Output Loading on Resistive Voltage Dividers, *October 1969*

☐ EB15 Low Input Resistance Voltage Dividers, *February 1970*

☐ EB17 Accuracy vs. Frequency of Models 290B and 250DE Universal Impedance Bridges, *(revised May 1969)*

☐ EB26 International System of Units, *August 1969*

☐ EB29 DC and Low Frequency AC Ratio Measurements, *Dr. Merle L. Morgan, September 1962*

☐ EB30 Traceability of Resistance Measurement, *Jack Riley, January 1964*

☐ EB34 Resistance Transfer Technique, *Lawrence H. White, (revised April 1968)*

☐ EB35 An Improved Technique for Establishing Resistance Ratios, *R. M. Pailthorp and J. C. Riley, November 1962*

☐ EB41 Derivation of Electrical Units from Fundamental Standards, *R. D. Kuykendall and R. M. Pailthorp, July 1964*

☐ EB44 DC measurements Using Ratio Techniques, *Jack C. Riley, September 1965*

☐ TA2 A Ratio Transformer Bridge for Standardization of Inductors and Capacitors, *D. L. Hillhouse and H. W. Kline, August 1960*

☐ TA6 The Accuracy of Series and Parallel Connections of Four-Terminal Resistors, *Jack C. Riley, April 1965*

☐ TA8 AC Measurements Using Ratio Techniques, *Jack C. Riley, May 1965*

☐ TA14 The Advantages of a Ten Kilohm Transportable Resistance Standard, *Robert M. Pailthorp, September 1967*

☐ TA16 Which Bridge for Precise Resistance Measurements? *Edward J. Swenson and George D. Vincent, December 1967*

☐ TA17 Experimental Verification of the Five-Terminal, Ten-Kilohm Resistor as a Device for Dissemination of the Ohm, *R. M. Pailthorp and George Vincent, December 1968*

☐ TA22A Laser Resistance Trimming from the Measurement Point of View, *Arthur G. Albin and Edward J. Swenson, June 1971*

☐ TA23 Precision Measurement of Resistor Networks, *Robert M. Pailthorp and Jack C. Riley, June 1971*

☐ TA24 Predictive Adjustment of Tantalum Film Resistors by Anodization, *Donald R. Cutler and Edward J. Swenson, July 1971*

☐ TA25 Laser Trimming Analysis Using a Resistive Sheet Analogy, *Swenson, Vincent, Riley, December 1972*

☐ TA26 The Effects of Laser Trimming on Birox and 1100 Series Thick Film Composition, *N. S. Spann, R. Headley, G. D. Vincent and E. J. Swenson, October 1971*

☐ TA27 Laser Trimming Thin Film Precision Resistor Networks with an Automated System, *Leonhard Groth, January 1974*

☐ TA28 YAG Laser Trimming of Thick Film Resistors, *Headley, Popowich, Anders, January 1974*

☐ TA31 A Method of Obtaining Optimum Trimming Performance from a Laser System, *Paul F. Parks and Thomas W. Richardson, October 1974*

☐ TA32 Laser Trimming RC Active Filters, *Edward J. Swenson, April 1978*

☐ TA33 Reducing Post Trim Drift of Thin Film Resistors By Optimizing YAG Laser Output Characteristics, *June 1978*

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